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CREATIVE IN TAIWAN

Software Proxy Memory Interface

SIGNAL, HARDWARE PLATFORM, PACKAGE, COMMAND SET, OPERATION TIME, AND TIMING DIAGRAM

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Contents

Software Proxy Memory Interface

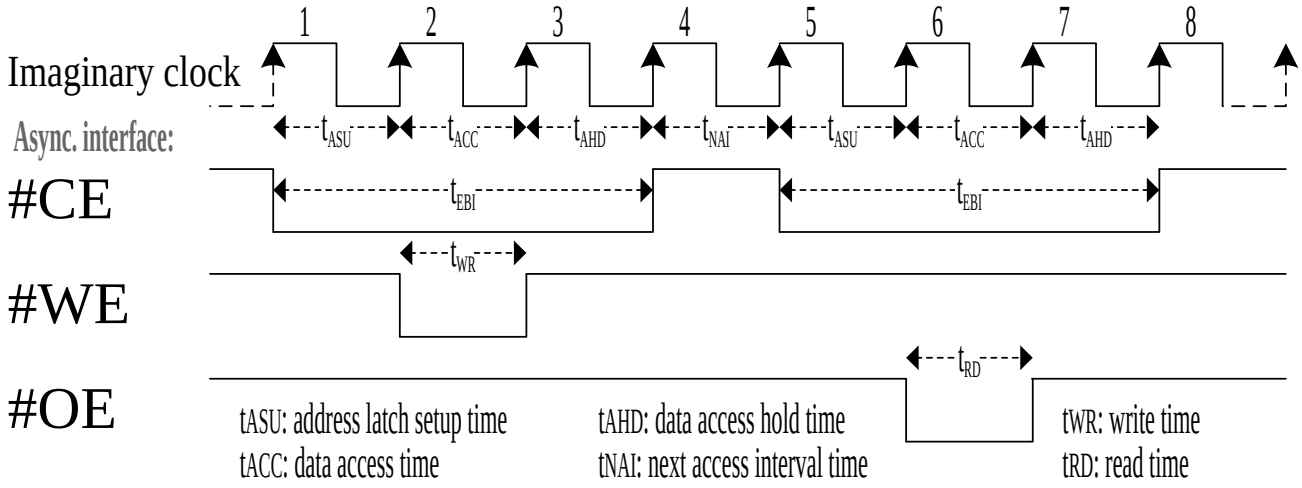
A software program executing in the microprocessor, it works in coordination with the external bus interface (EBI) or the internal interconnect bus to access and control various memories. The memory comprises DRAM and the flash memory. The software program can be a firmware, a microcode, or implemented in the FPGA.

Software Proxy Memory Interface (SPMI)

- ***The technical terms of major EBI signals:***

A[a]	address bus, said 'a' is address width
D[d]	data bus, said 'd' is data width
#CS; #CE	chip selection on the host side; chip enable on the device side
#WE	write enable
#OE	output enable

Timing Diagram of EBI



$$t_{EBI} = t_{ASU} + t_{ACC} + t_{AHD}$$

$$Bus\ Frequency = \frac{1}{t_{EBI} + t_{NAI}} \| Bus\ Frequency \leq 200MHz$$

$$Random\ Access\ Cycle = t_{EBI} + t_{NAI}$$

$$Burst\ Access\ Cycle = t_{ACC} + t_{NAI}$$

- ***The time parameters for DRAM:***

Data Retention Time on the Cell: tDRC

Average Periodic Refresh Interval: tREFI (refer to DDR-n SDRAM specification)

Refresh Cycle Time: tRFC (refer to DDR-n SDRAM specification)

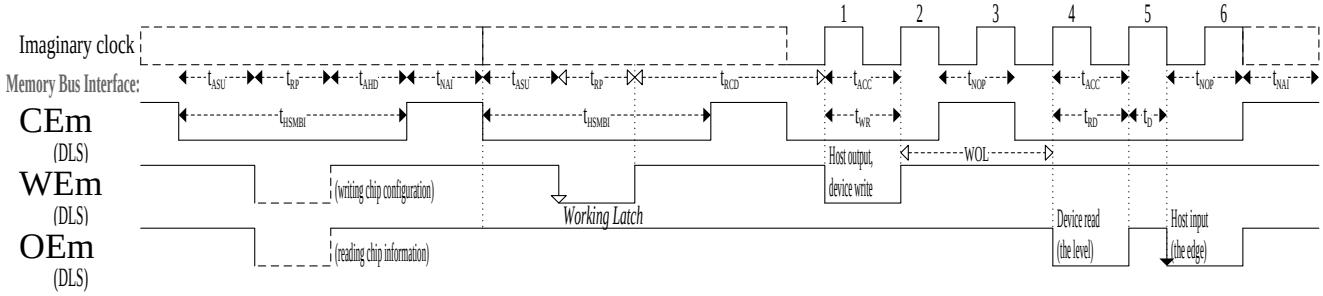
Write One Latency: WOL

High Speed Memory Bus Interface (HSMBI)

The high-speed memory bus interface using a high-speed transmission hardware to speed up accessing main memory. The interface is based on the external bus interface, and improving the timing sequence to enhance performance.

The signals on the interface are used a class of Low Voltage Differential Logic Signal (LVDLS); the address bus and the data bus are used a type of Low Voltage Logic Signal (LVLS); the access signals are used a type of Differential Logic Signal (DLS), or the LVLS.

Timing Diagram of HSMBI



➢ Symbol and Definition:

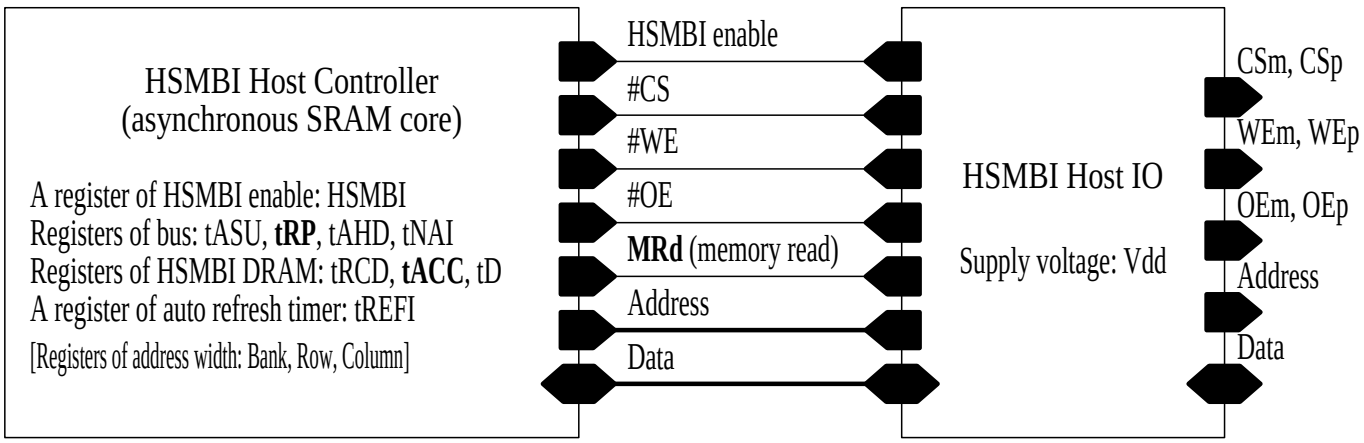
tASU	address latch setup time	tWR	write time	tRCD	row to column delay time
tRP	register/precharge time	tRD	read time	tNOP	no operation time
tAHD	data access hold time	tACC	data access time	WOL	write one latency
tNAI	next access interval time	tD	gate and wire delay time		

$$t_{HSMBI} = t_{ASU} + t_{RP} + t_{AHD}$$

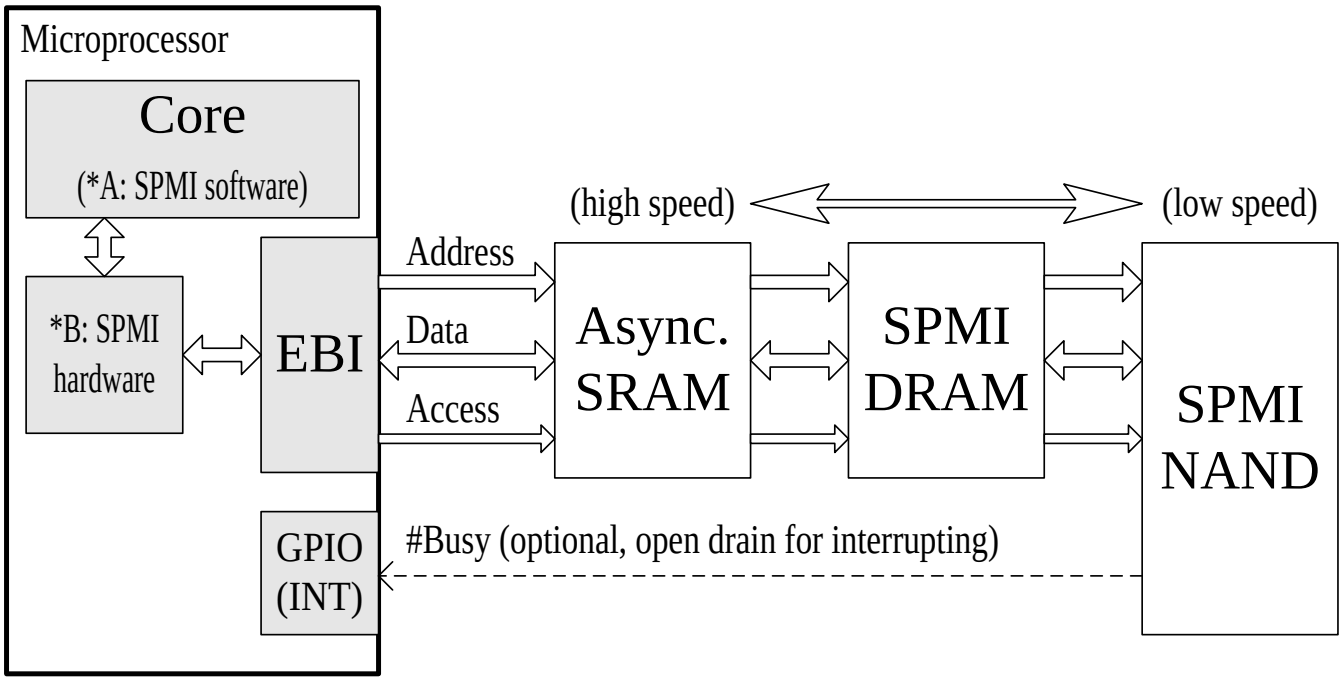
$$Bus\ Frequency = \frac{1}{t_{HSMBI} + t_{NAI}} \| Bus\ Frequency \geq 100MHz$$

$$Memory\ Access\ Cycle = t_{ACC} + t_D$$

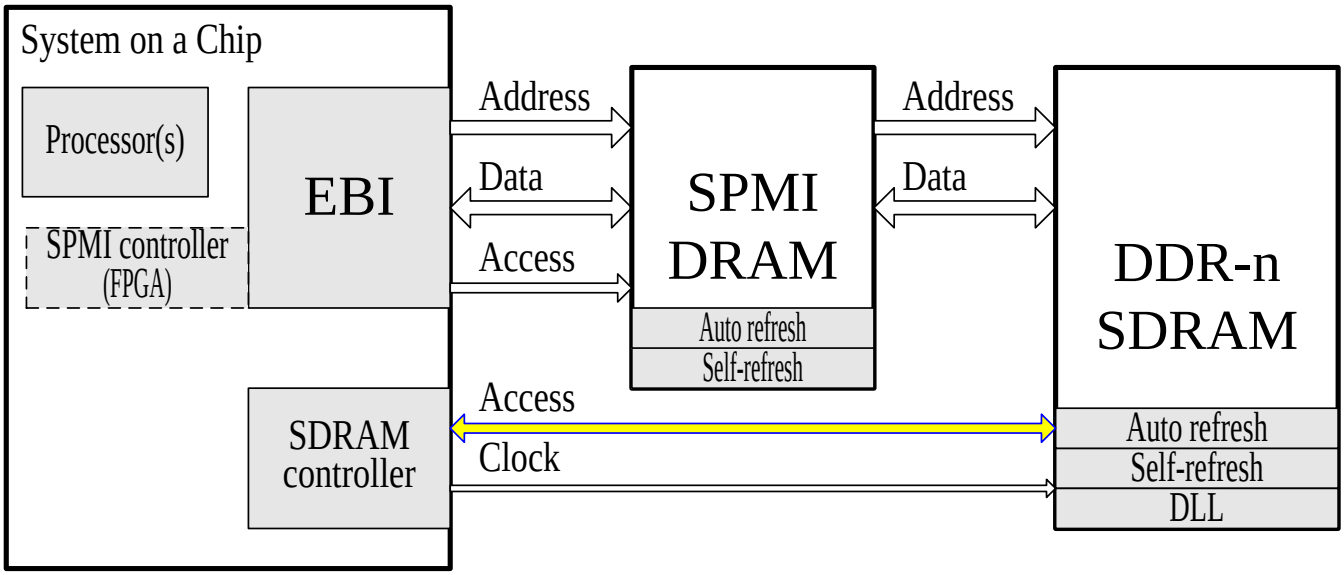
HSMBI Host Controller and IO



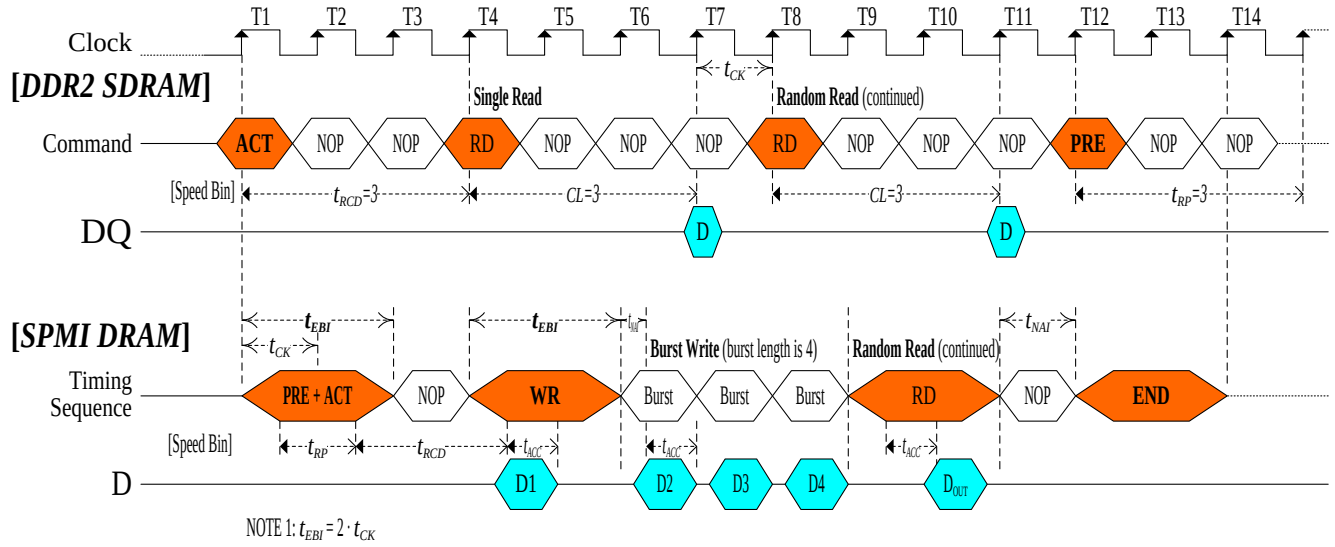
Hardware Platform Architecture



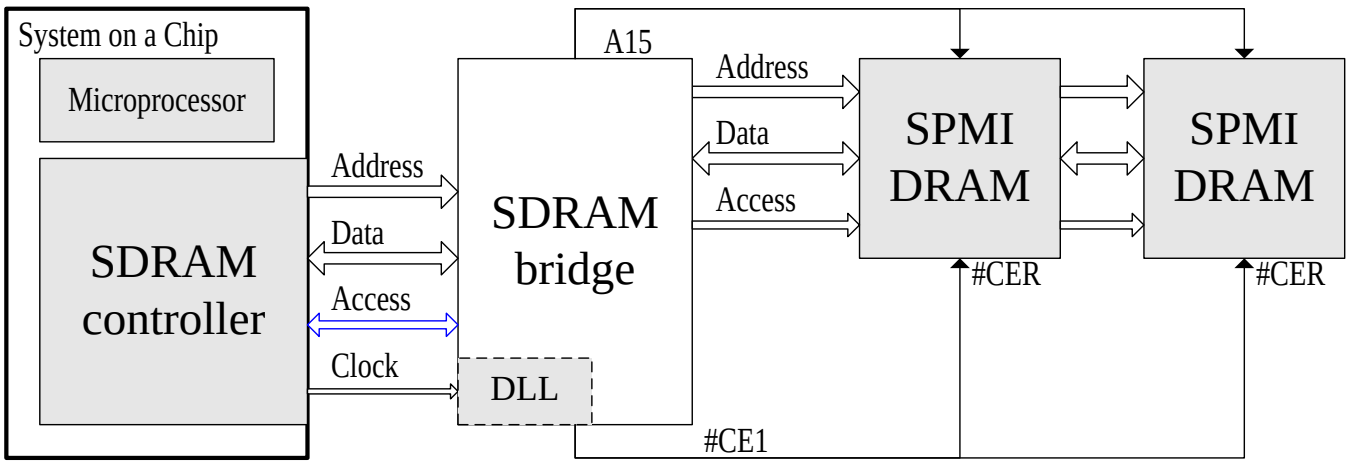
SPMI DRAM versus DDR-n SDRAM



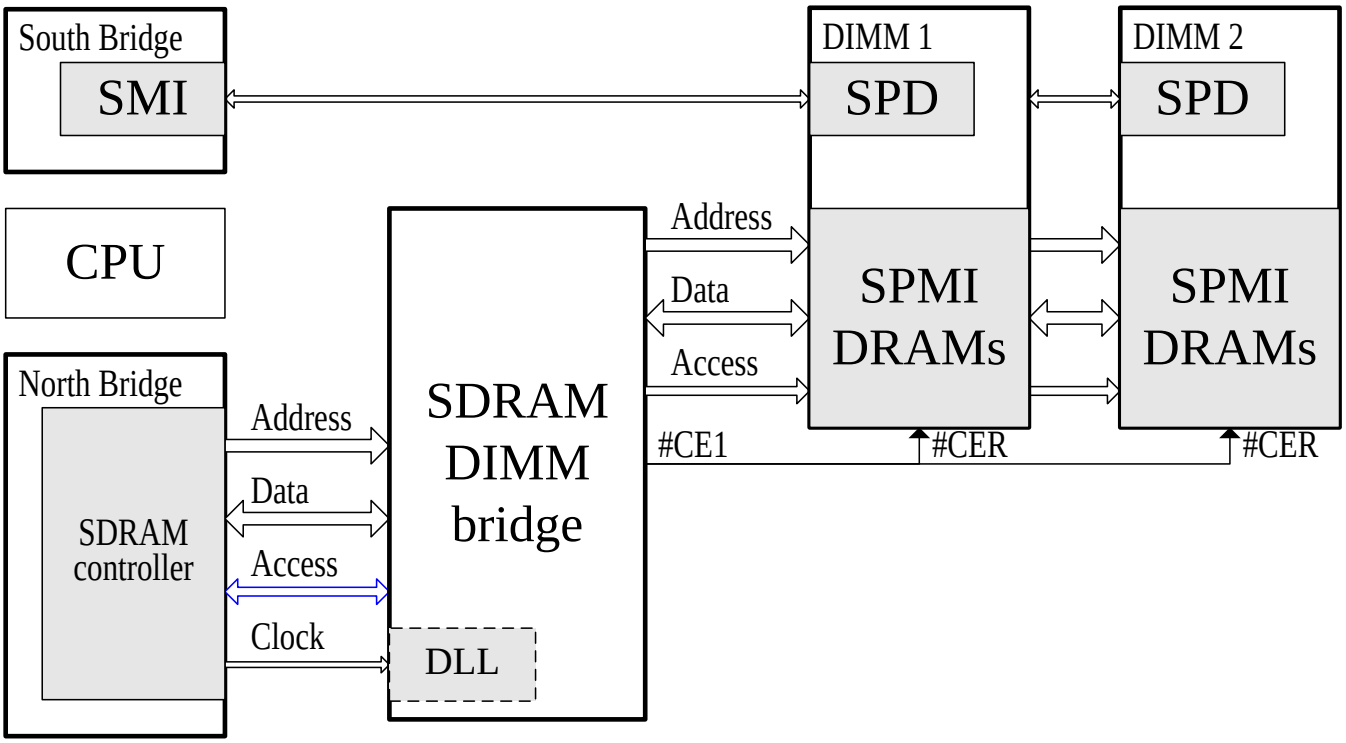
SPMI DRAM versus DDR2 SDRAM



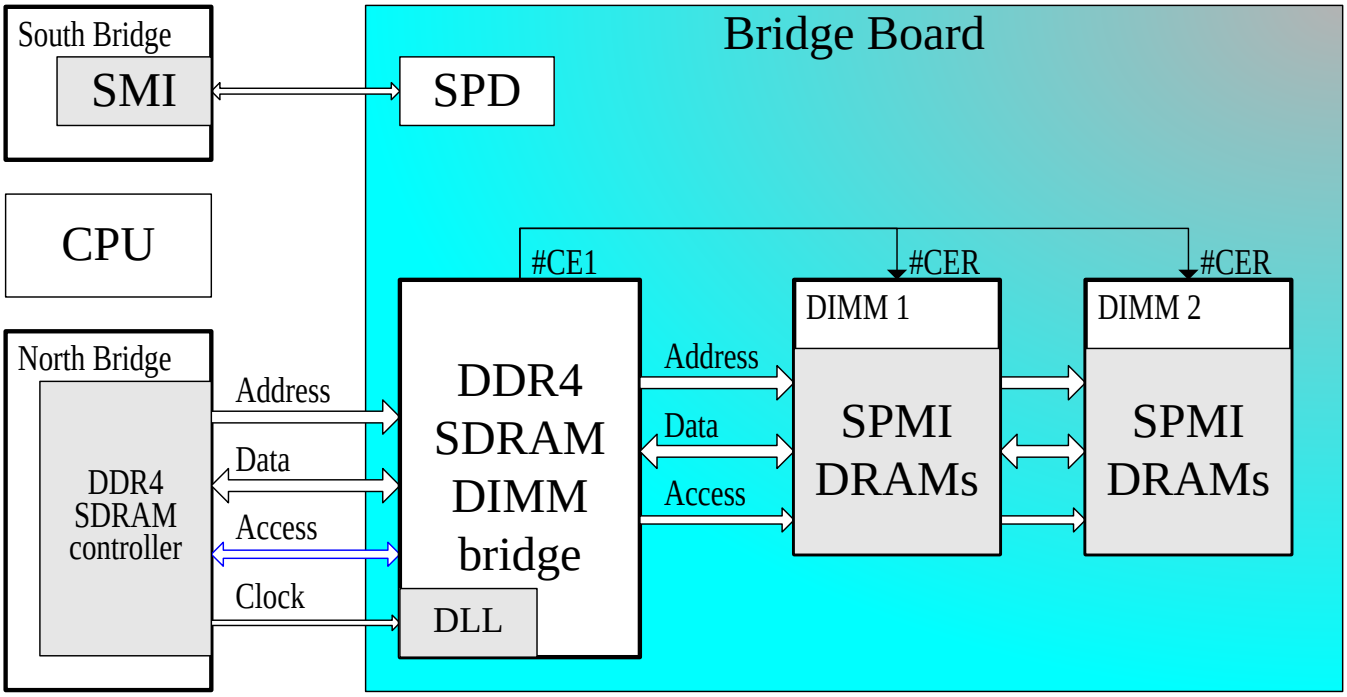
SDRAM Bridge: hardware platform of SoC



SDRAM DIMM Bridge: hardware platform of X86 personal computer



SDRAM DIMM Bridge Board: hardware platform of X86 personal computer



Package Ball-out

DDR2 SDRAM package mapping table

The package ball-out please refer to “JEDEC STANDARD, DDR2 SDRAM SPECIFICATION”.

Input/output of DDR2 SDRAM interface on the device side, and mapping to SPMI

Symbol of DDR2 SDRAM	**Type of DDR2 SDRAM**	**Symbol of SPMI DRAM**	**Type of SPMI DRAM**	**Symbol of SPMI NAND**	**Type of SPMI NAND**
A0—A15 (address bus)	Input	A0—A15 (address bus)	Input	AD0—AD15	Input / Output
DQ (data bus)	Input / Output	D (data bus)	Input / Output	(reserved)	
CK, #CK	Input	(reserved)		(reserved)	
CKE	Input	(reserved)		**ALE**	Input
#CS	Input	#CE	Input	#CE	Input
DM	Input	#OE	Input	#OE	Input
#WE	Input	#WE	Input	#WE	Input
#RAS	Input	#CER	Input	(reserved)	
#CAS	Input	(reserved)		[#Busy]	Output (open drain)
ODT	Input	ST (self-test)	Input	ST (self-test)	Input
[#UDQS]	Input / Output	[#UB]	Input	[#UB]	Input
[#LDQS]	Input / Output	[#LB]	Input	[#LB]	Input
#RESET	Input	#RESET	Input	#RESET	Input
V_{REF}	Supply	[V_{PP}]	Supply	[V_{PP}]	Supply
V_{DDQ}	Supply	V_{DDQ}	Supply	V_{DDQ}	Supply
V_{SSQ}	Supply	V_{SSQ}	Supply	V_{SSQ}	Supply
V_{DD}	Supply	V_{DD}	Supply	V_{DD}	Supply
V_{SS}	Supply	V_{SS}	Supply	V_{SS}	Supply

Input/output of SPMI DRAM on the device side, and mapping to EBI DRAM

Symbol of SPMI DRAM	Type of SPMI DRAM	Symbol of EBI DRAM	Type of EBI DRAM
A0—A15 (address bus)	Input	AD0—AD15 (address and data bus)	Input / Output
D (data bus)	Input / Output	(reserved)	
(reserved)		(reserved)	
(reserved)		ALE	Input
#CE	Input	#CE	Input
#OE	Input	#OE	Input
#WE	Input	#WE	Input
#CER	Input	(reserved)	
(reserved)		(reserved)	
ST (self-test)	Input	ST (self-test)	Input
[#UB]	Input	[#UB]	Input
[#LB]	Input	[#LB]	Input
#RESET	Input	#RESET	Input
[V_{PP}]	Supply	[V_{PP}]	Supply
V_{DDQ}	Supply	V_{DDQ}	Supply
V_{SSQ}	Supply	V_{SSQ}	Supply
V_{DD}	Supply	V_{DD}	Supply
V_{SS}	Supply	V_{SS}	Supply

DDR3 SDRAM package mapping table

The package ball-out please refer to “JEDEC STANDARD, DDR3 SDRAM SPECIFICATION”.

Input/output of DDR3 SDRAM interface on the device side, and mapping to SPMI

Symbol of DDR3 SDRAM	**Type of DDR3 SDRAM**	**Symbol of SPMI DRAM**	**Type of SPMI DRAM**	**Symbol of SPMI NAND**	**Type of SPMI NAND**
A0—A15 (address bus)	Input	A0—A15 (address bus)	Input	AD0—AD15	Input / Output
DQ (data bus)	Input / Output	D (data bus)	Input / Output	(reserved)	
CK, #CK	Input	(reserved)		(reserved)	
CKE	Input	(reserved)		**ALE**	Input
#CS	Input	#CE	Input	#CE	Input
DM	Input	#OE	Input	#OE	Input
#WE	Input	#WE	Input	#WE	Input
#RAS	Input	#CER	Input	(reserved)	
#CAS	Input	(reserved)		[#Busy]	Output (open drain)
ODT	Input	ST (self-test)	Input	ST (self-test)	Input
[#DQSU]	Input / Output	[#UB]	Input	[#UB]	Input
[#DQSL]	Input / Output	[#LB]	Input	[#LB]	Input
#RESET	Input	#RESET	Input	#RESET	Input
V_{REFDQ}, V_{REFCA}	Supply	[V_{PP}]	Supply	[V_{PP}]	Supply
V_{DDQ}	Supply	V_{DDQ}	Supply	V_{DDQ}	Supply
V_{SSQ}	Supply	V_{SSQ}	Supply	V_{SSQ}	Supply
V_{DD}	Supply	V_{DD}	Supply	V_{DD}	Supply
V_{SS}	Supply	V_{SS}	Supply	V_{SS}	Supply

Input/output of DDR3 SDRAM interface on the device side, and mapping to HSMBI DRAM

Symbol of DDR3 SDRAM	Type of DDR3 SDRAM	Symbol of HSMBI DRAM	Type of HSMBI DRAM
A0—A15 (address bus)	Input	A0—A15 (address bus)	Input (LVLS)
DQ (data bus)	Input / Output	D (data bus)	Input / Output (LVLS)
CK, #CK	Input	CEm, CEp (#CE)	Differential Input (DLS)
CKE	Input	(reserved)	
#CS0, #CS1	Input	CERm, CERp (#CER)	Differential Input (DLS)
#CS2, #CS3	Input	(reserved)	
DQSU, #DQSU	Input / Output	OEm, OEp (#OE)	Differential Input (DLS)
DQSL, #DQSL	Input / Output	WEm, WEp (#WE)	Differential Input (DLS)
#WE	Input	[#UB/B1]	Input (LVLS)
#RAS	Input	[#LB/B0]	Input (LVLS)
#CAS	Input	[B3]	Input (LVLS)
ODT	Input	[B2]	Input (LVLS)
#RESET	Input	#RESET	Input
V_{REFDQ}, V_{REFCA}	Supply	[V_{PP}]	Supply
V_{DDQ}	Supply	V_{DDQ}	Supply
V_{SSQ}	Supply	V_{SSQ}	Supply
V_{DD}	Supply	V_{DD}	Supply
V_{SS}	Supply	V_{SS}	Supply

SPMI DRAM

Applying to a high performance dynamic random-access memory.

Parameters of speed bin: tRP or tACC (use the bigger value to suit the interface), tRCD

- ***Symbols***

Address width of bank: b

Address width of row: r (r≤14)

Address width of column: c (c<r)

Mount of storage cell: n

Operation Time of Accessing and Refreshing

- ***The device refresh parameters***

tDRC: decided by the struct of the storage cell, the process technology, and the 'n'

$$t_{REFI} = \frac{t_{DRC}}{n} \| n = 2^x, x \geq 7$$

$$t_{RFC} \cong t_{RP} + t_{RCD} + t_{ACC} + t_{NOP} + t_{NAI} \| gate\ delay$$

- ***The time of random access (tRACC) with data amount (DA)***

$$t_{RACC} = t_{RCD} + t_{NAI} * DA + t_{EBI} * (2 + DA)$$

- ***The time of burst access (tBACC) with data amount (DA)***

$$t_{BACC} = t_{RCD} + t_{NAI} * DA + t_{EBI} * 3 + t_{ACC} * (DA - 1)$$

Command Set

Function	A[15:14]	A[r-1:0]	D[7:0]
Data Access	01	Column Address*1	Byte
Single Bank Precharge, Random Access	01	Row Address	Bank Address
Single Bank Precharge, Synchronization Burst Access*2	01	Row Address	Bank Address
Function End	00	X	X
Read Chip Information	00	Page Number	V (hardware fixed)
Write Chip Configuration	00	Page Number	V (power on reset)
Auto Refresh (all bank)	10	Activating #CER*3	

NOTE 1: the device first receives the row address, and then receives the column address (A[c-1:0]) after.

NOTE 2: rolling column address.

NOTE 3: several #CER (#CE for refresh) connect to same #CE to be a refresh group.

Chip Information

D[7:5]	D[4:3]	D[2:1]	D[0]	A[2]=0, A[1:0]
Number of banks 000: 2 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 256	**Pins of row** 00: 11 01: 12 10: 13 11: 14	**Width of column** 00: 10 | 6(LP) 01: 11 | 7(LP) 10: 12 | 8(LP) 11: 13 | 9(LP)	**Low power activity** 0: normal 1: LP	**Info. Page** 00: page 0

D[7:6]	D[4:0]	A[2]=0, A[1:0]
Mount of storage cell 00: 128 01: 256 10: 512 11: 1024	**Null** 0	**Info. Page** 01: page 1

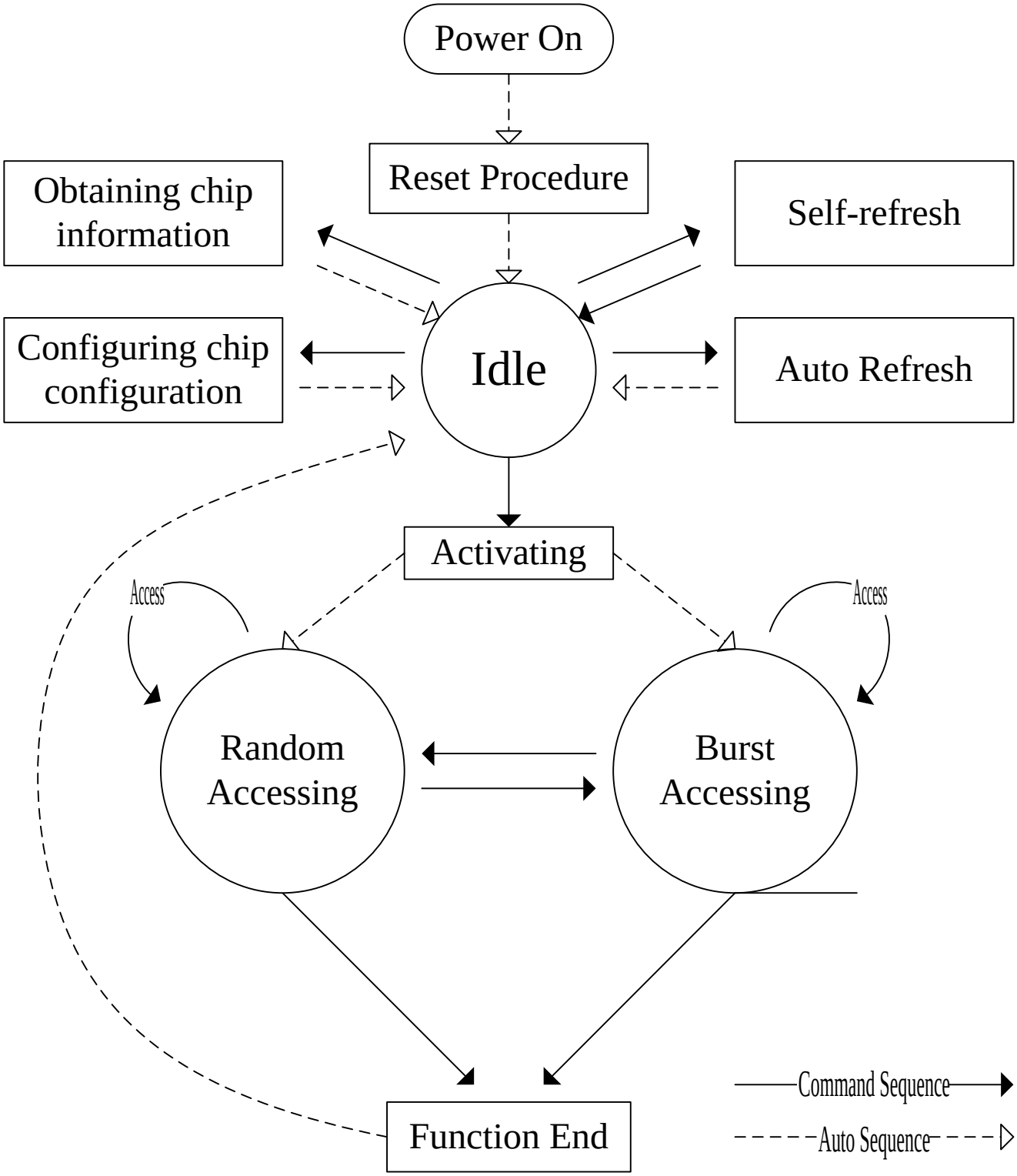
Chip Configuration

D[7:1]	D[0]	A[2]=0, A[1:0]
Null 0	**Self-refresh** 0: exit (POR) 1: entry	**Config page** 00: page 0

Bank Refresh Mask

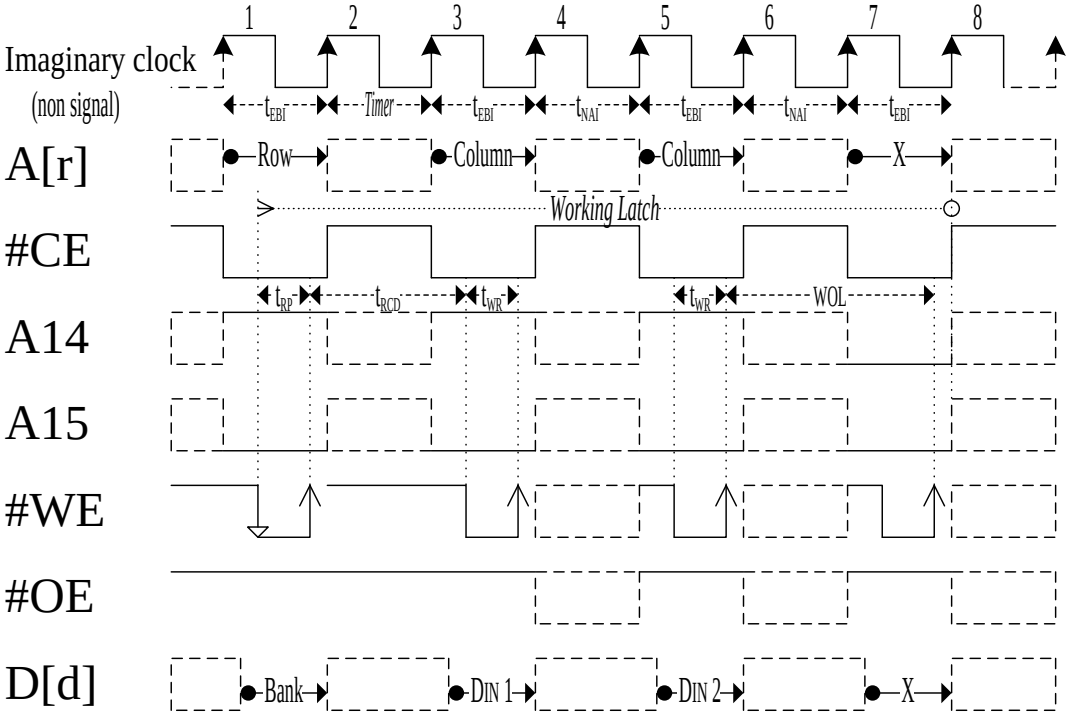
D[7:0]	A[7:3], A[2]=1
Mask bits (for low power application only, and masks bank 0 to bank 255) 0: the indicated bank will not refresh 1: normal (POR)	**Mask page** XXXXX: 0 to 31

Simplified State Diagram

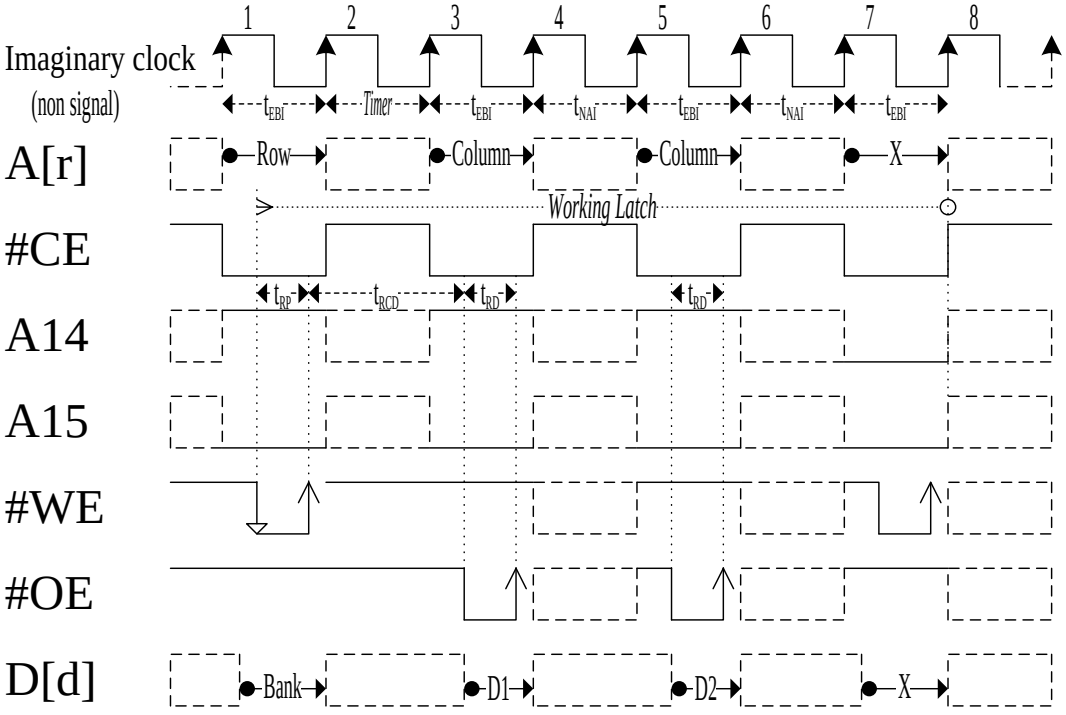


Timing Diagram

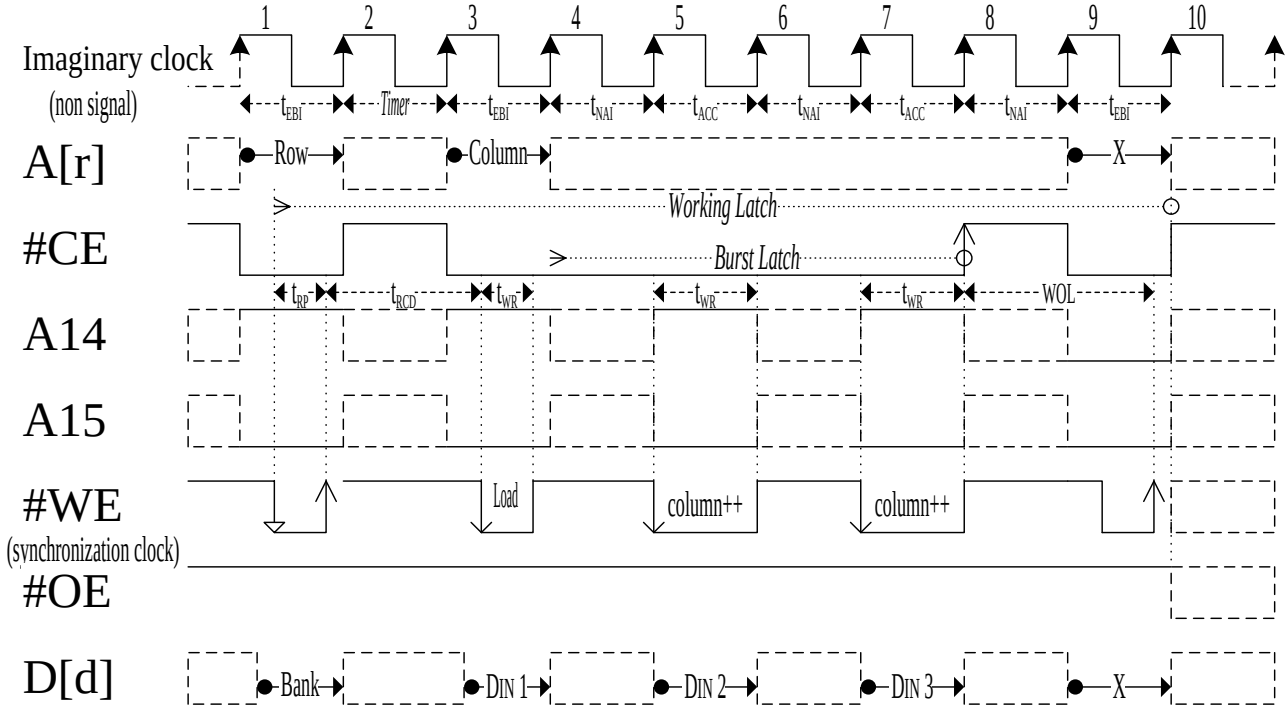
- Random Write



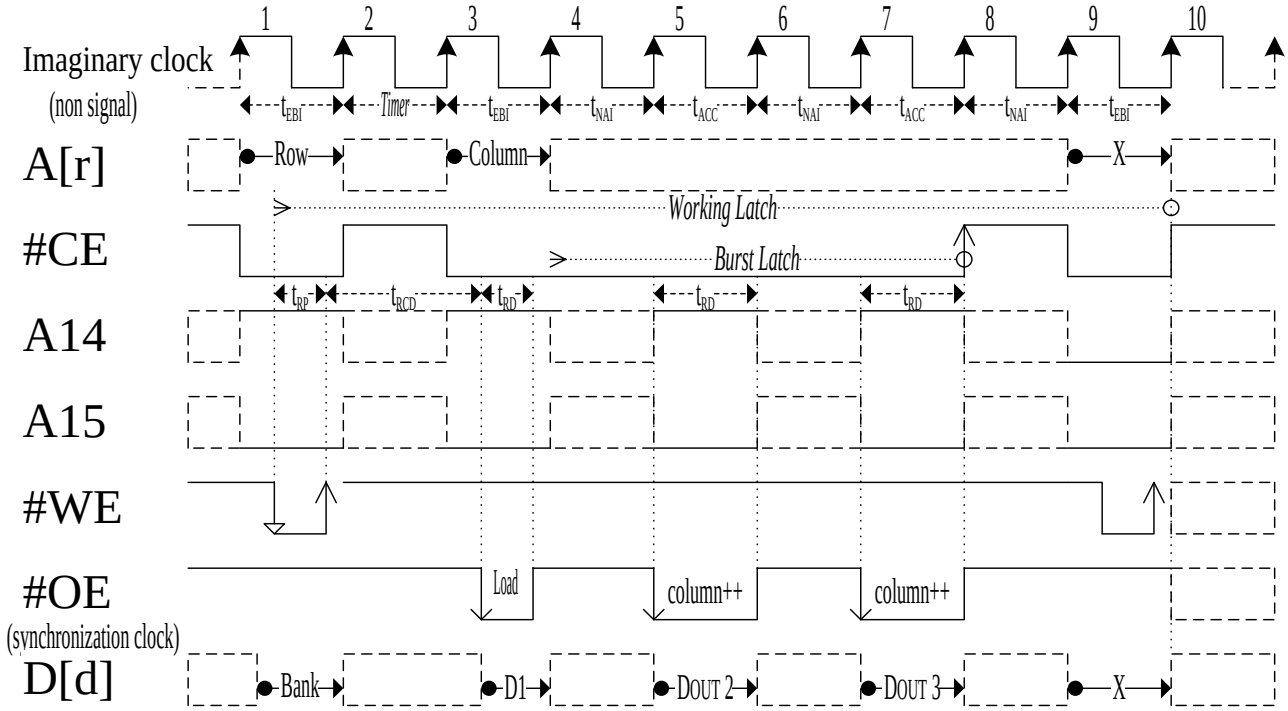
- Random Read



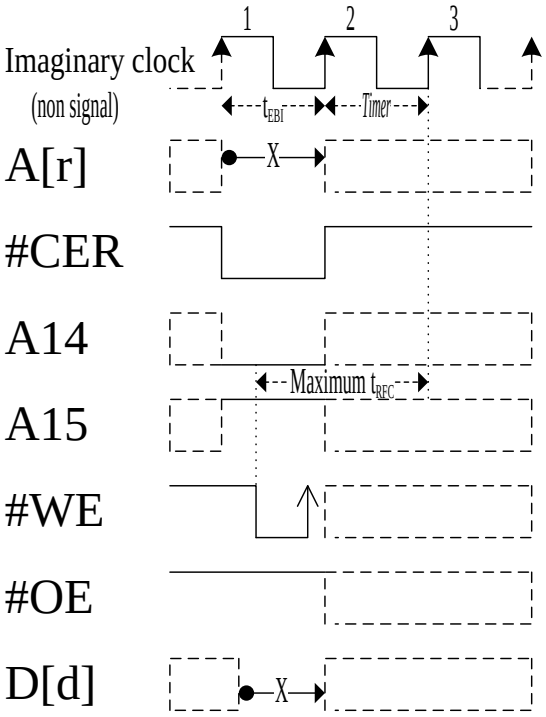
■ Synchronization Burst Write



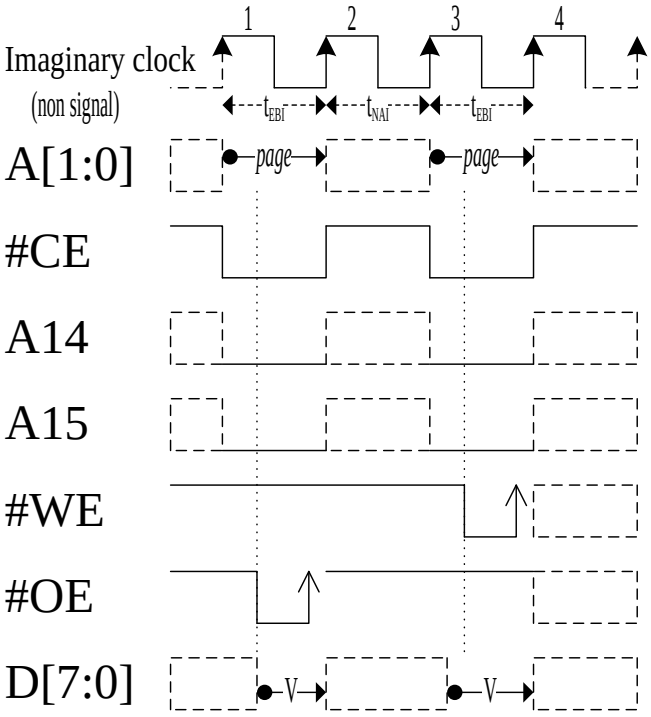
■ Synchronization Burst Read



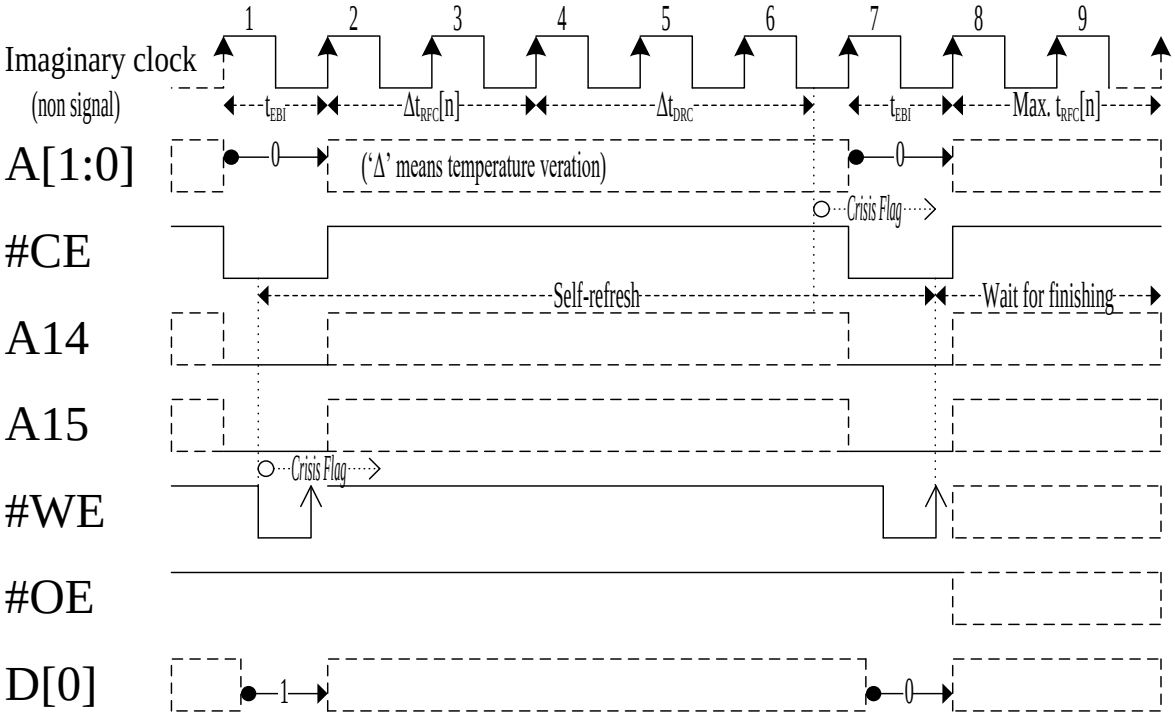
- Auto Refresh



- Chip Information and Chip Configuration



■ Self-Refresh Entry and Self-Refresh Exit



HSMBI DRAM

Applying to a high performance and high-speed transmission dynamic random-access memory.

Parameters of speed bin: tRP, tRCD, tACC

Other items please refer to SPMI DRAM.

Operation Time of Accessing and Refreshing

The device refresh parameters

Please refer to SPMI DRAM.

The time of memory access (tMACC) with data amount (DA)

$$t_{MACC} = t_{RCD} + t_{NAI} + t_{HSMBI} * 2 + (t_{ACC} + t_{\mathrm{D}}) * DA$$

Command Set

Function	A[15:14]	A[r-1:0]	D[7:0]
Data Access	01	Column Address*1	Byte
Single Bank Precharge, Device Access*2	01	Row Address	Bank Address
Function End	00	X	X
Read Chip Information	00	Page Number	V (hardware fixed)
Write Chip Configuration	00	Page Number	V (power on reset)
Auto Refresh (all bank)	10	Activating #CER*3	
NOTE 1: the device first receives the row address, and then receives the column address (A[c-1:0]) after. NOTE 2: random or burst is the same. NOTE 3: several #CER (#CE for refresh) connect to same #CE to be a refresh group.			

Chip Information

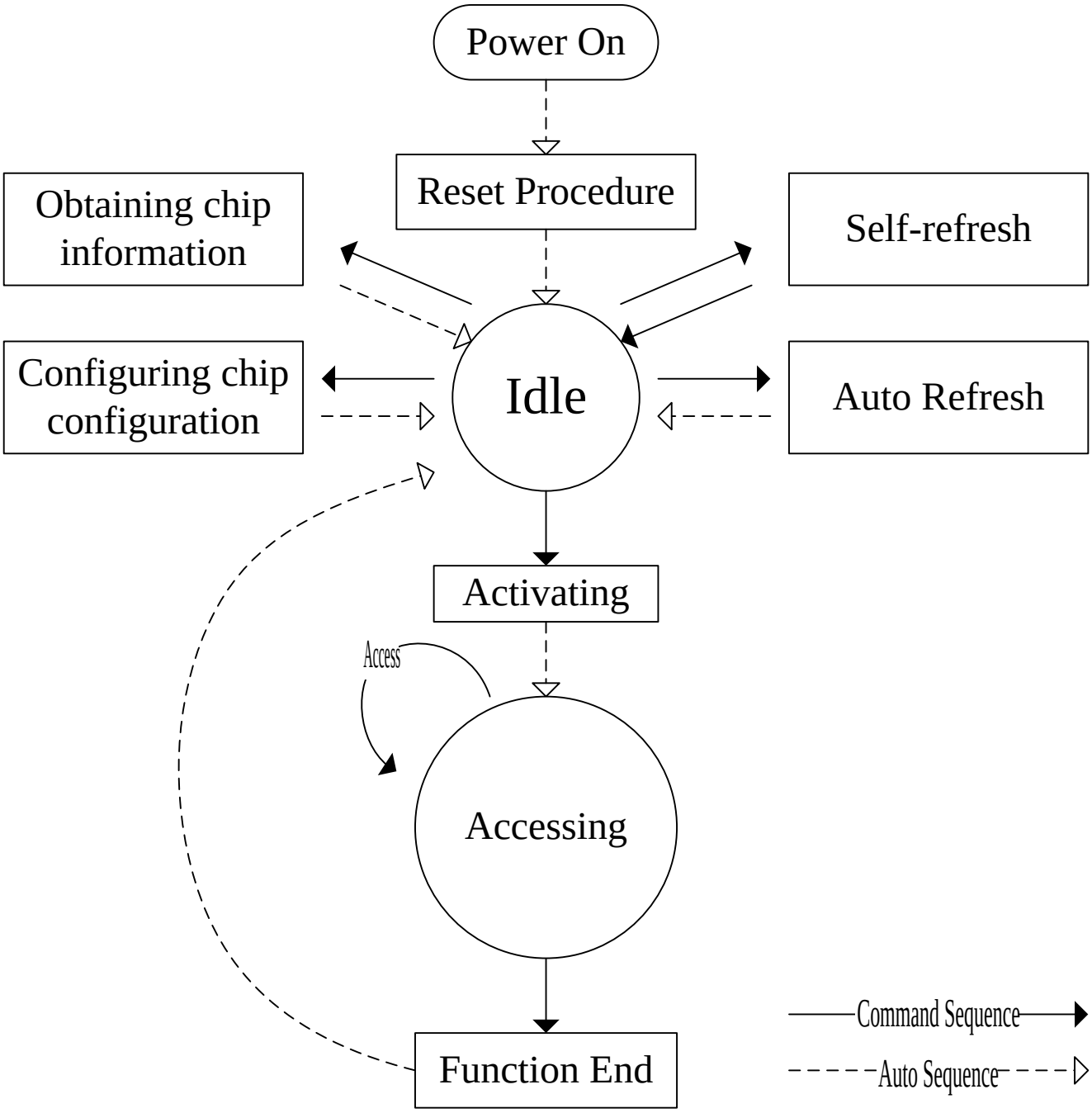
Please refer to SPMI DRAM.

Chip Configuration

Please refer to SPMI DRAM.

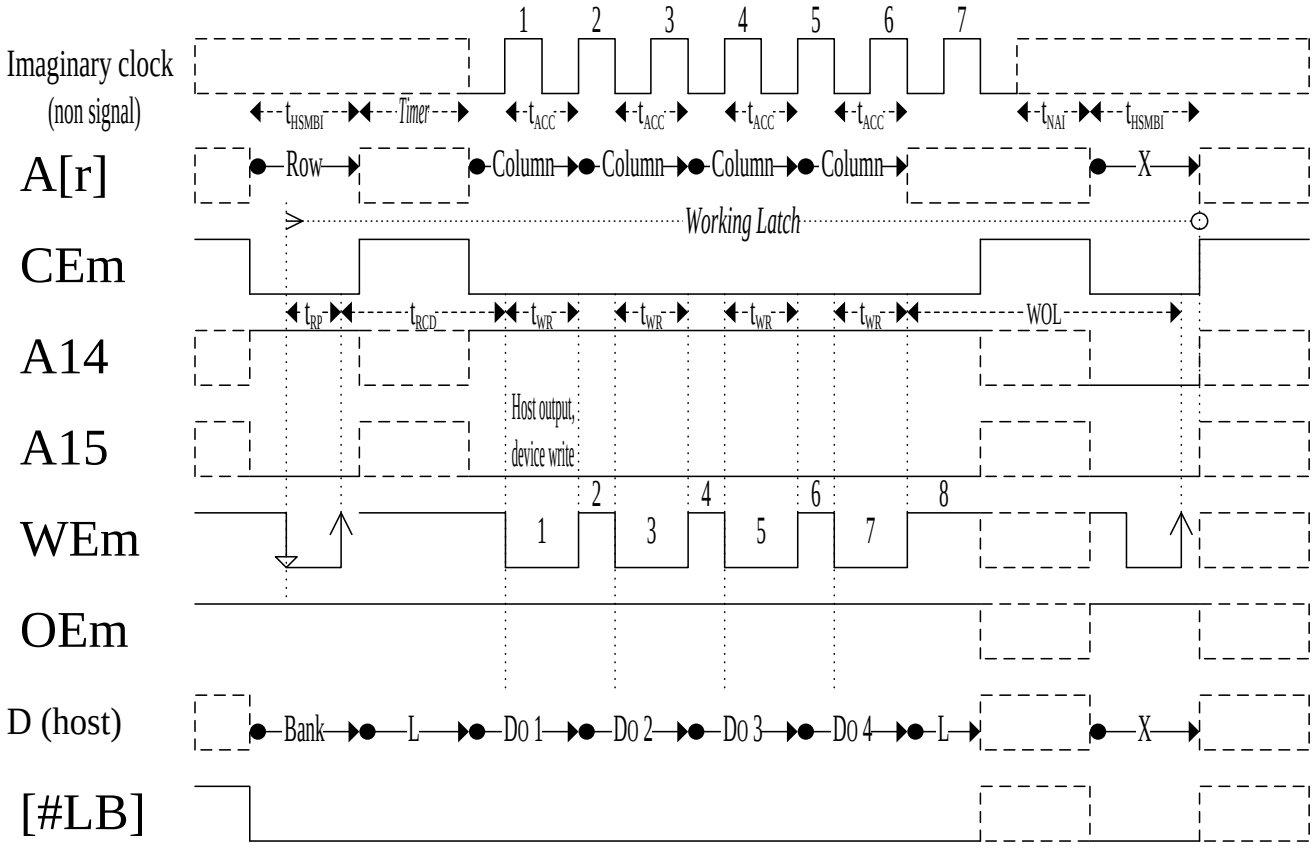
D[7:1]	D[0]	A[2]=0, A[1:0]
Null 0	**Self-test** 0: normal work (POR) 1: self-test (a pulse)	**Config page** 11: page 3

Simplified State Diagram

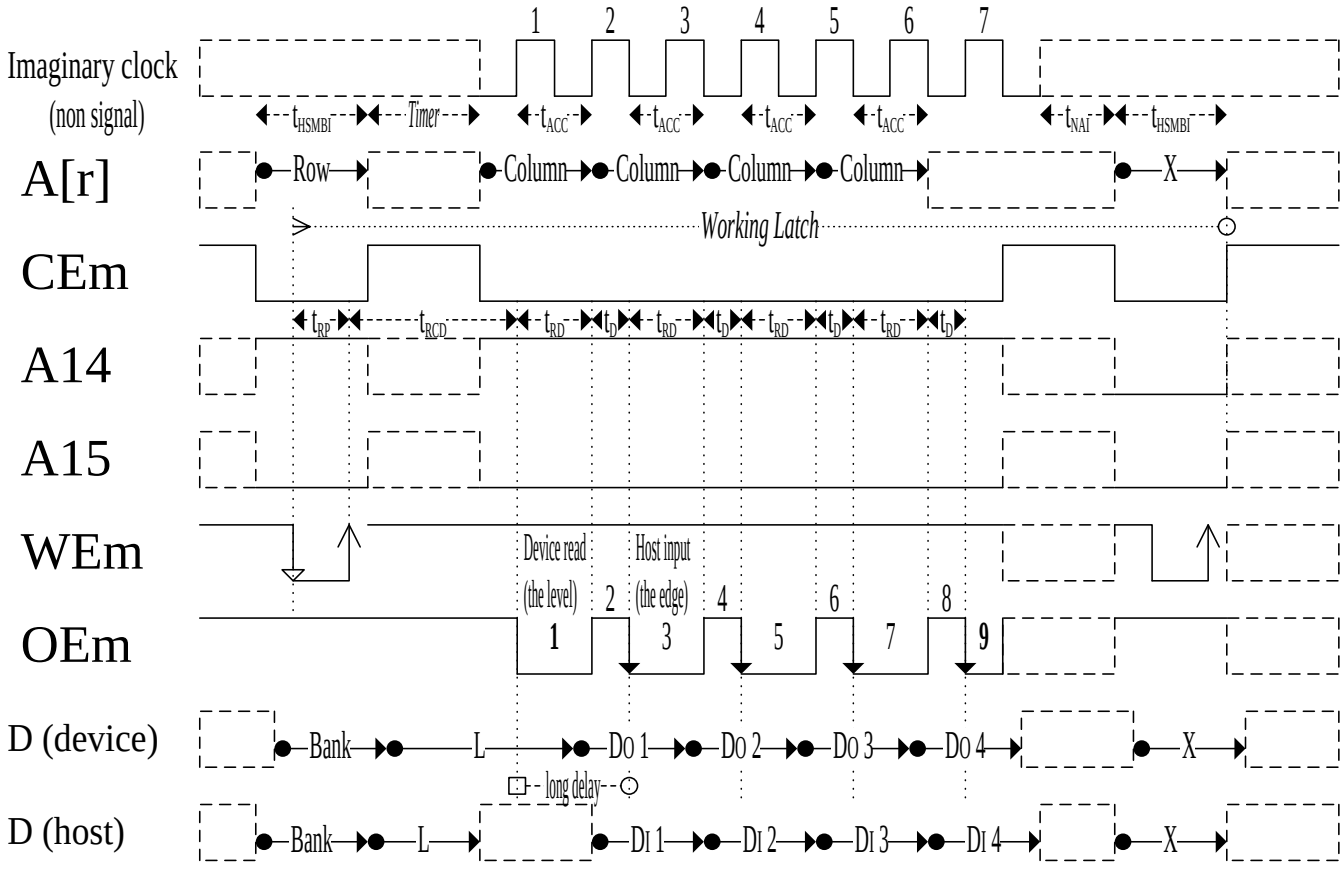


Timing Diagram

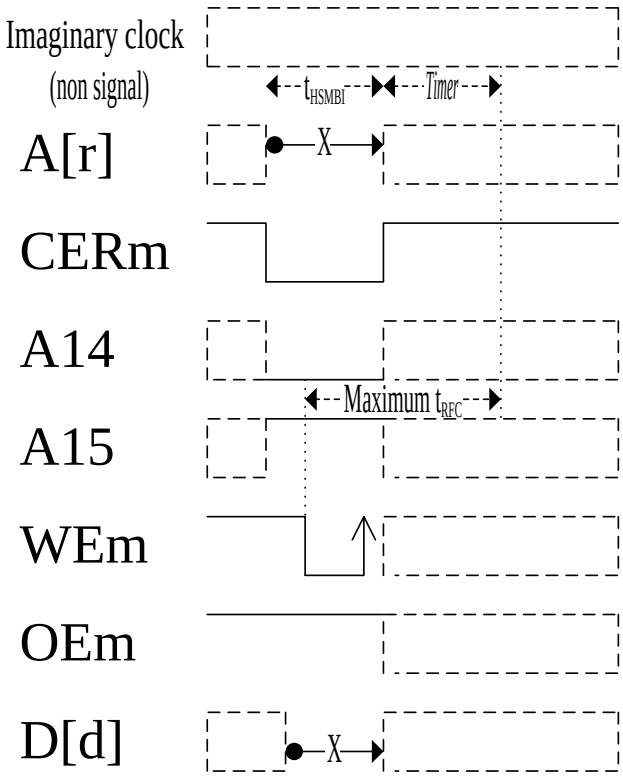
- Write



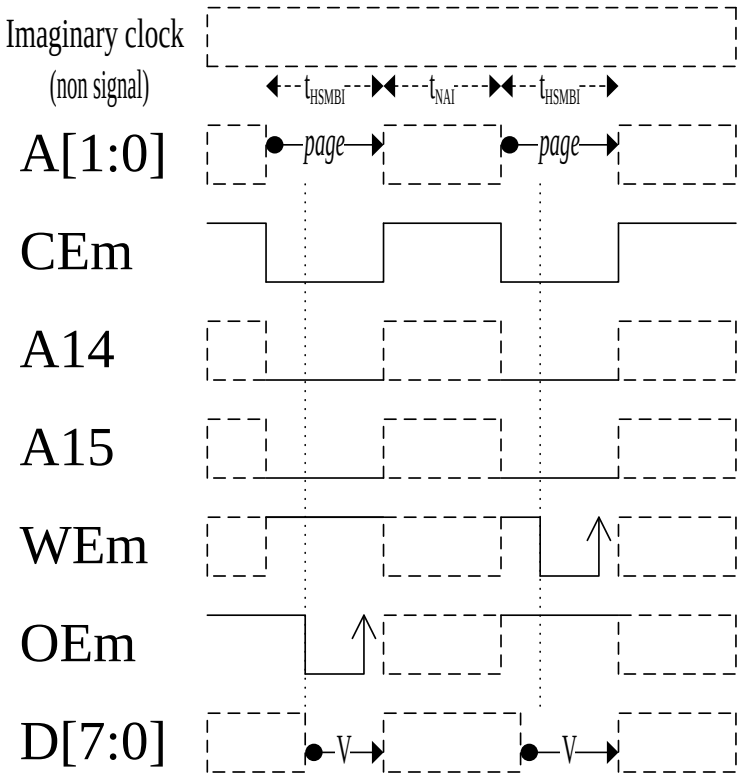
- Read



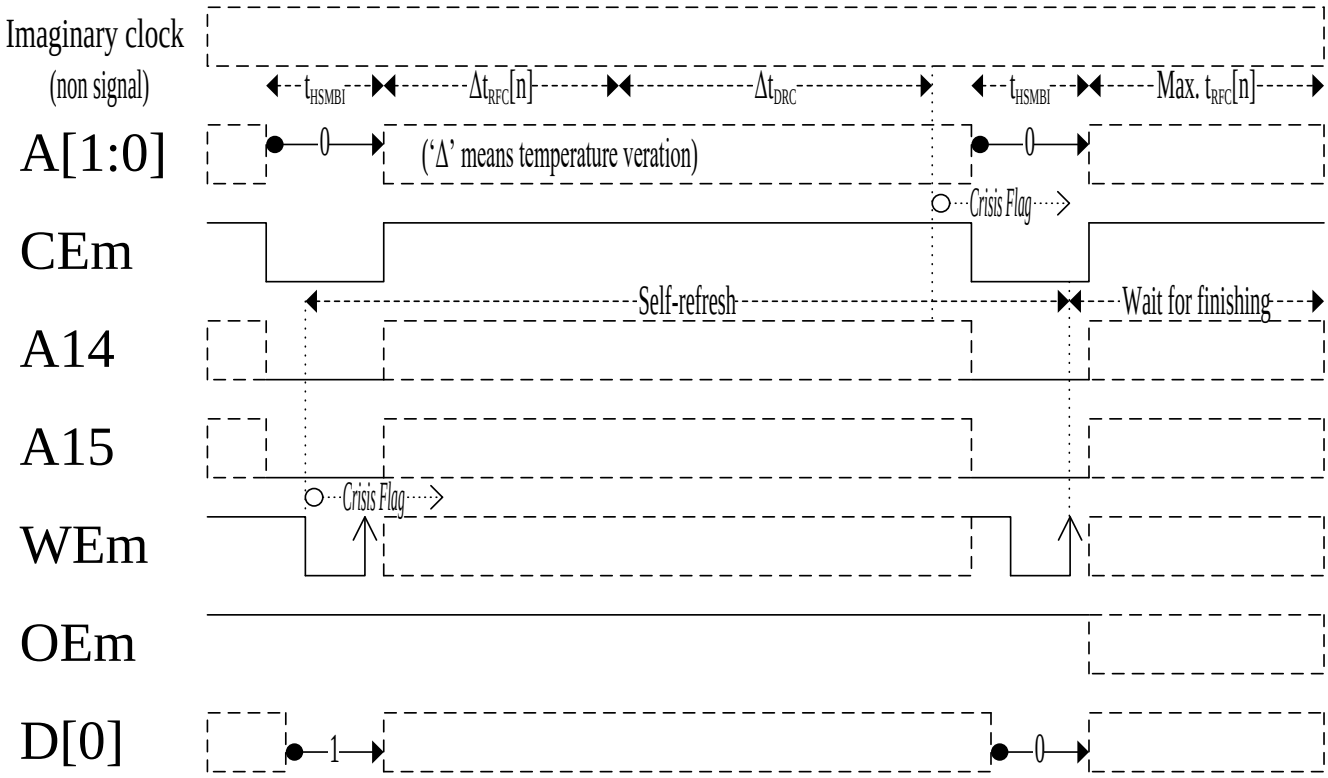
- Auto Refresh



- Chip Information and Chip Configuration



■ Self-Refresh Entry and Self-Refresh Exit



EBI DRAM

Applying to a dynamic random-access memory without refresh command. Its interface is low pin count, and it such likes as the pseudo-SRAM, but the performance is higher.

Other items please refer to SPMI DRAM.

Operation Time of Accessing

- ***The device refresh parameters***

Please refer to SPMI DRAM.

- ***The time of random access (tRACC) with data amount (DA)***

$$t_{RACC} = t_{RFC} + t_{RCD} + t_{NAI} * DA + t_{EBI} * (2 + DA)$$

- ***The time of burst access (tBACC) with data amount (DA)***

$$t_{BACC} = t_{RFC} + t_{RCD} + t_{NAI} * DA + t_{EBI} * 3 + t_{ACC} * (DA - 1)$$

Command Set

Function	A[15:14]	A[r-1:0]	D[7:0]
Single Bank Precharge; Random Access; Function End	01 01 00	Row Address Column Address*1 X	Bank Address Byte X
Single Bank Precharge; Synchronization Burst Access*2; Function End	01 01 00	Row Address Column Address X	Bank Address Byte X
Read Chip Information	00	Page Number	V (hardware fixed)
Write Chip Configuration	00	Page Number	V (power on reset)
NOTE 1: the device first receives the row address, and then receives the column address (A[c-1:0]) after. NOTE 2: rolling column address.			

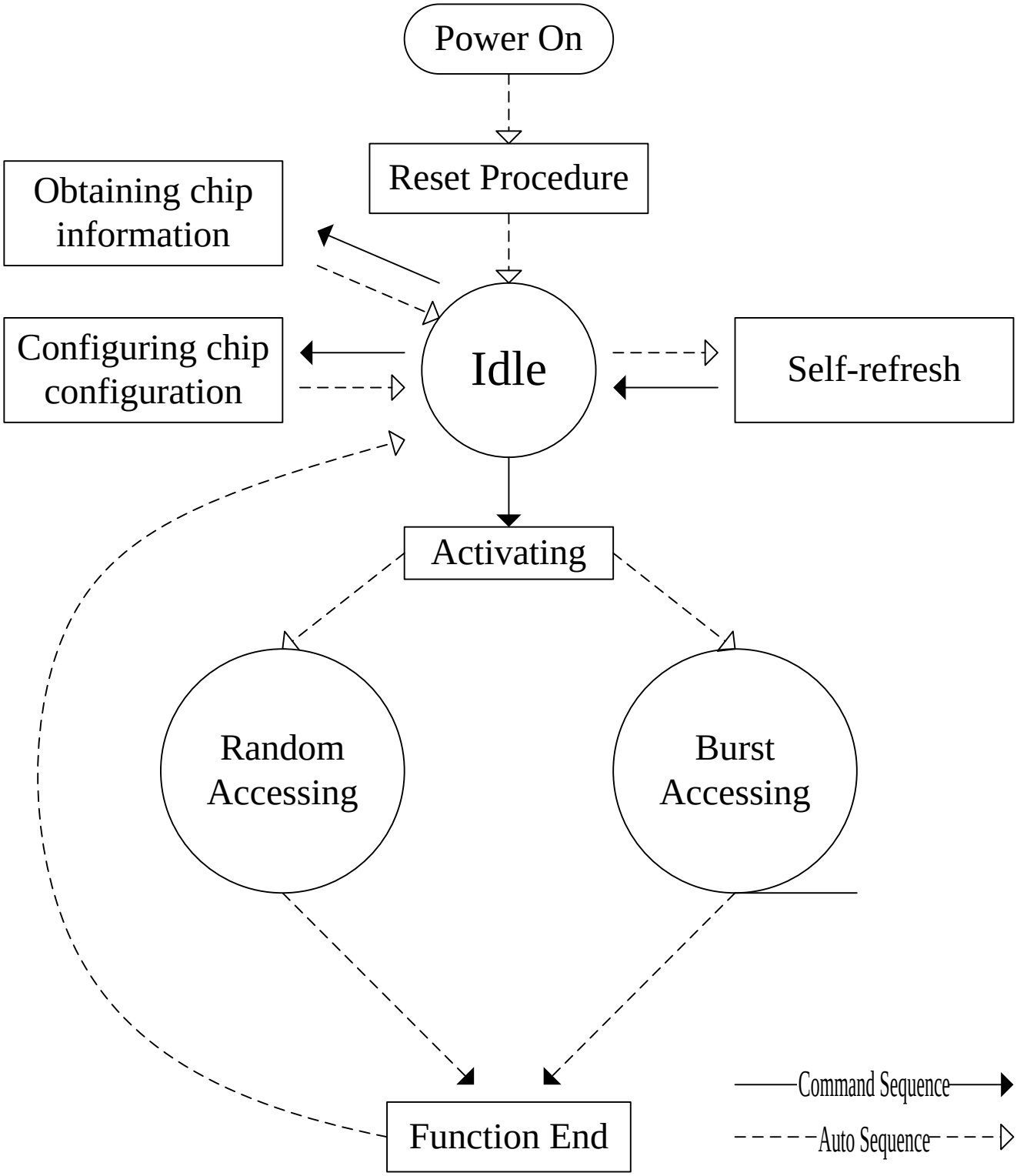
Chip Information

Please refer to SPMI DRAM.

Chip Configuration

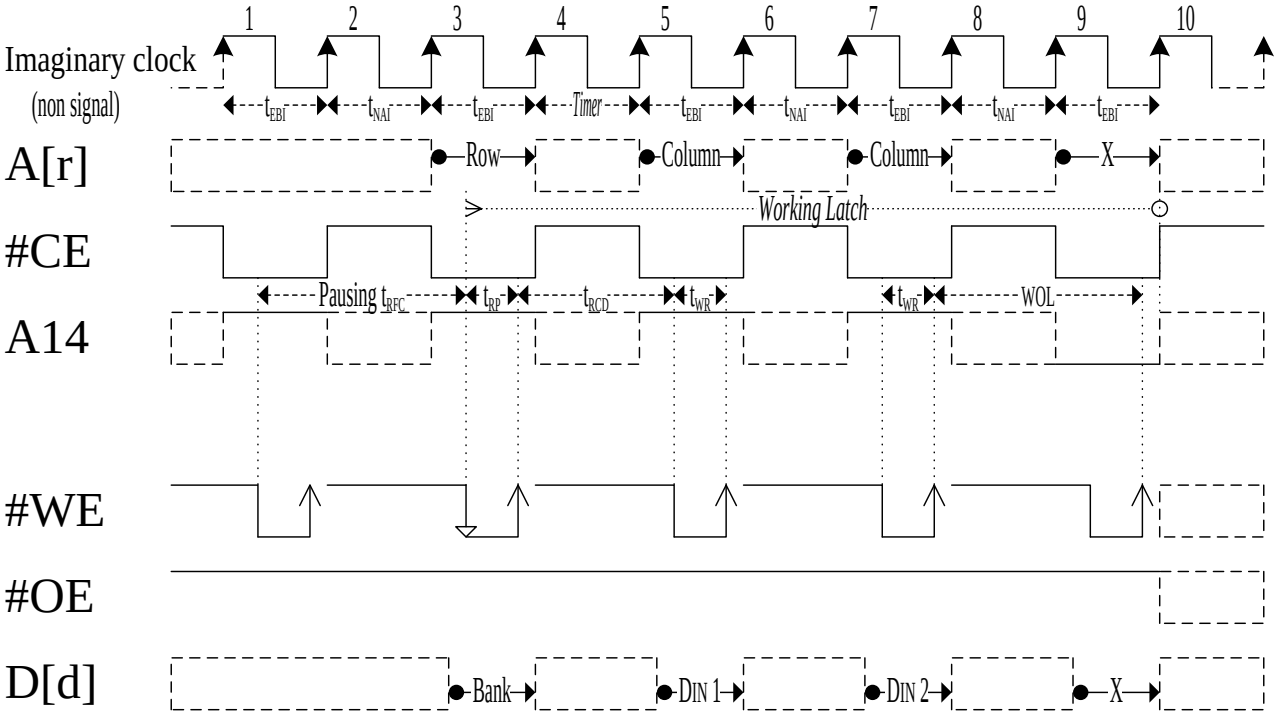
Please refer to SPMI DRAM, this chip configuration removes the self-refresh configuration.

Simplified State Diagram

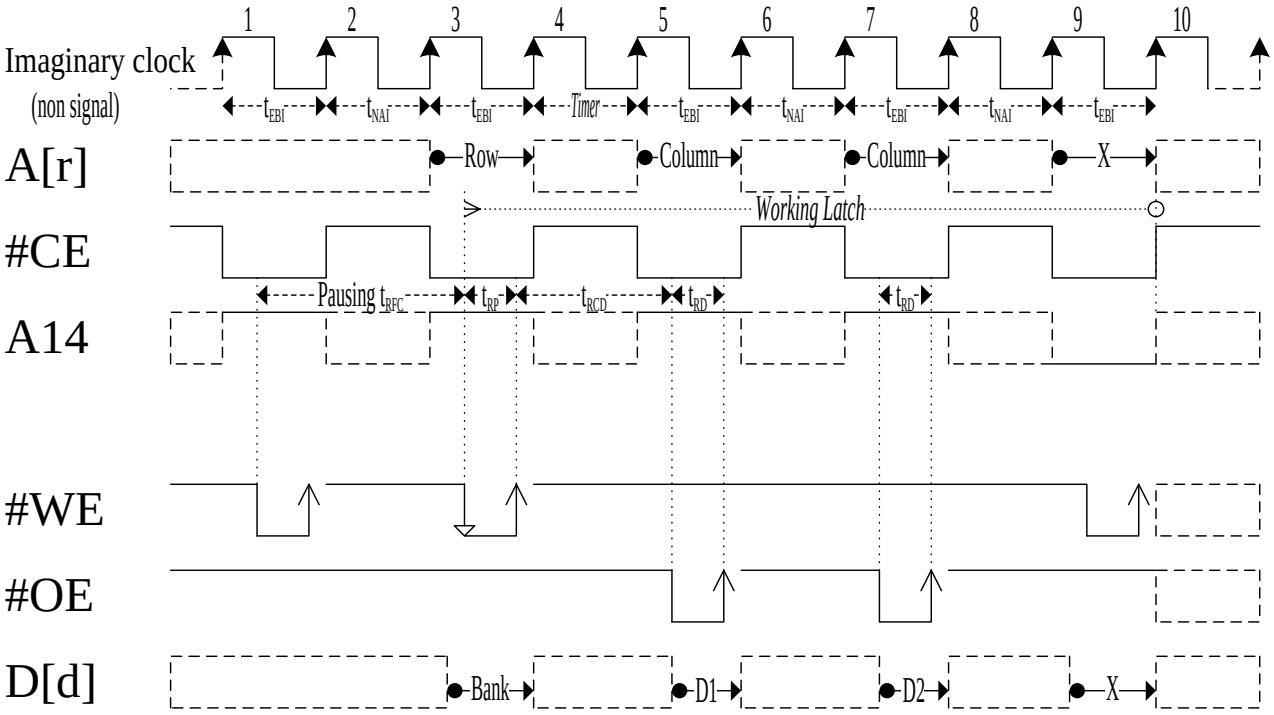


Timing Diagram

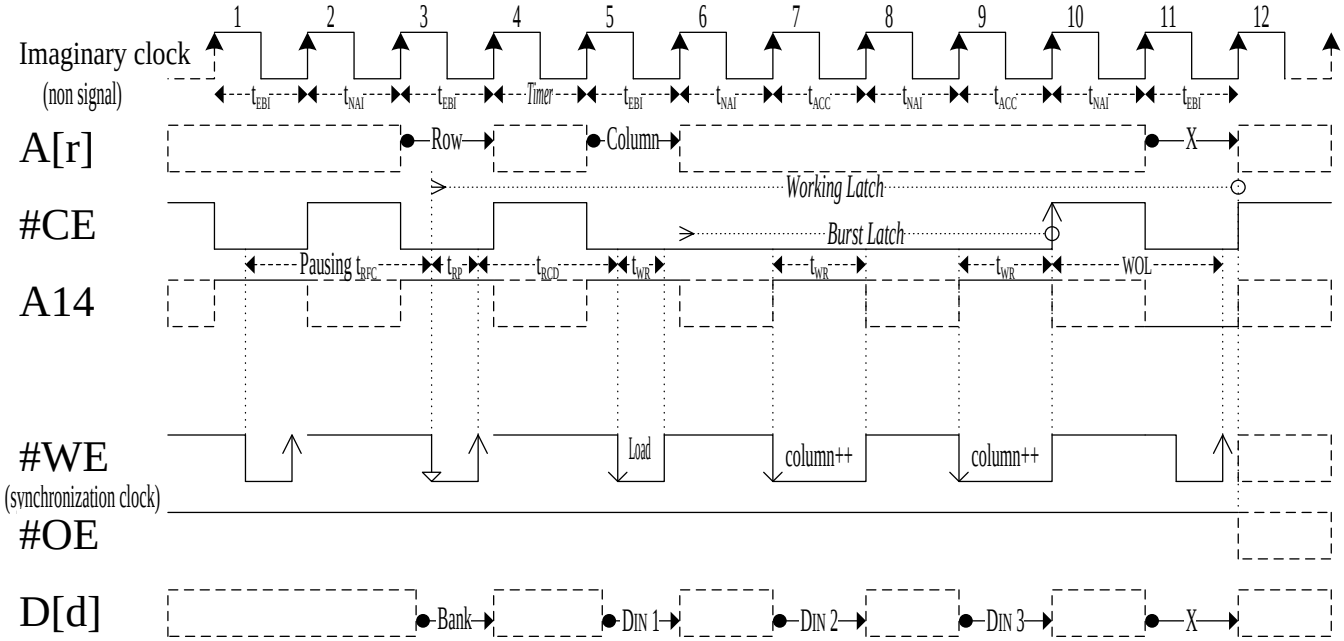
- Random Write



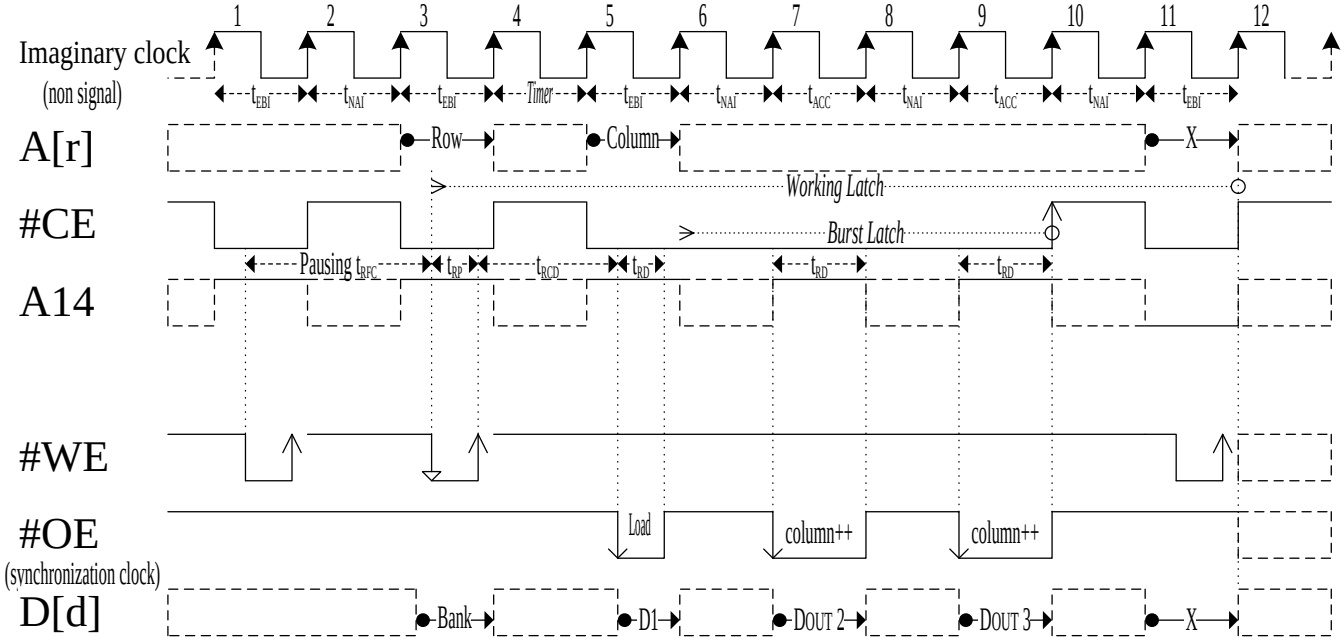
- Random Read



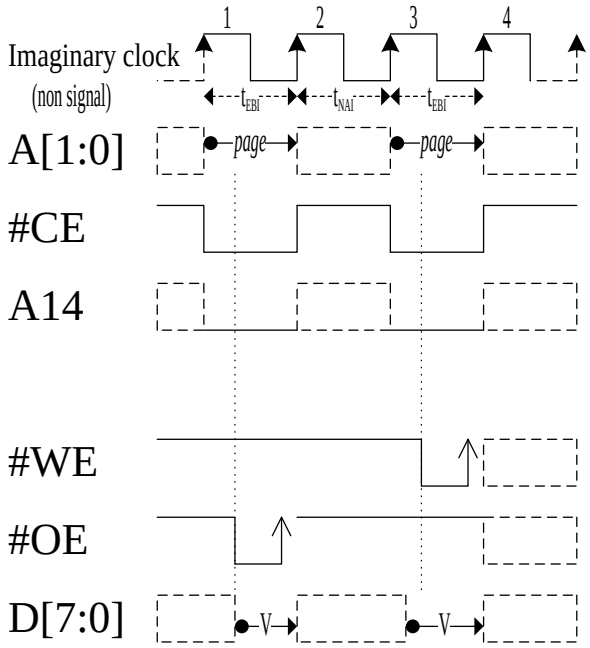
■ Synchronization Burst Write



■ Synchronization Burst Read



- Chip Information and Chip Configuration



SPMI NAND

Applying to the flash memory of NAND type.

Command Set

Function	A[15]	A[14:0]	D[7:2]	D[1:0]
Data Access	1	Column Address*1	Byte	
Random Access	1	Block, A[1:0]=00	LUN, Plane	0
Synchronization Burst Access*2	1	Block, A[1:0]=01	LUN, Plane	0
Block Erase (one block)	1	Block, A[1:0]=10	LUN, Plane	0
Block Erase all Planes	1	Block, A[1:0]=11	LUN, X	0
Page Read / Page Program (one page)	1	Block, Page	LUN, Plane	1 / 2
Page Read all Planes / Page Program all Planes	1	Block, Page	LUN, D[2]=0 / 1	3
Function End	0	X	X	
Read Chip Information	0	Page Number	V	
Write Chip Configuration	0	Page Number	V (power on reset)	
NOTE 1: the device first receives the block and page address, and then receives the column address after. NOTE 2: rolling column address.				

Chip Information

D[7:5]	D[4:2]	D[1:0]	A[2]=0, A[1:0]
Size of a page, and a block	**Number of blocks**	**Number of LUN**	**Info. Page**
000: 256, 64KB (legacy)	000: 16	00: 1 (legacy)	00: page 0
001: 512, 128KB	001: 32	01: 2	
010: 1024, 256KB	010: 64	10: 4	
011: 2048, 512KB	011: 128	11: 8	
100: 4096, 1024KB	100: 256		
101: 8192, 2048KB	101: 512		
110: 16384, 4096KB	110: 1024		
111: 32768, 8192KB	111: 2048		

D[7:6]	D[0]	A[2]=0, A[1:0]
Number of planes	**Null**	**Info. Page**
00: 1 (legacy)	0	01: page 1
01: 2		
10: 4		
11: 8		

D[7:6]	D[0]	A[2]=0, A[1:0]
Null 0	**Busy status** 0: ready (POR) 1: busy	**Info. Page** 11: page 3

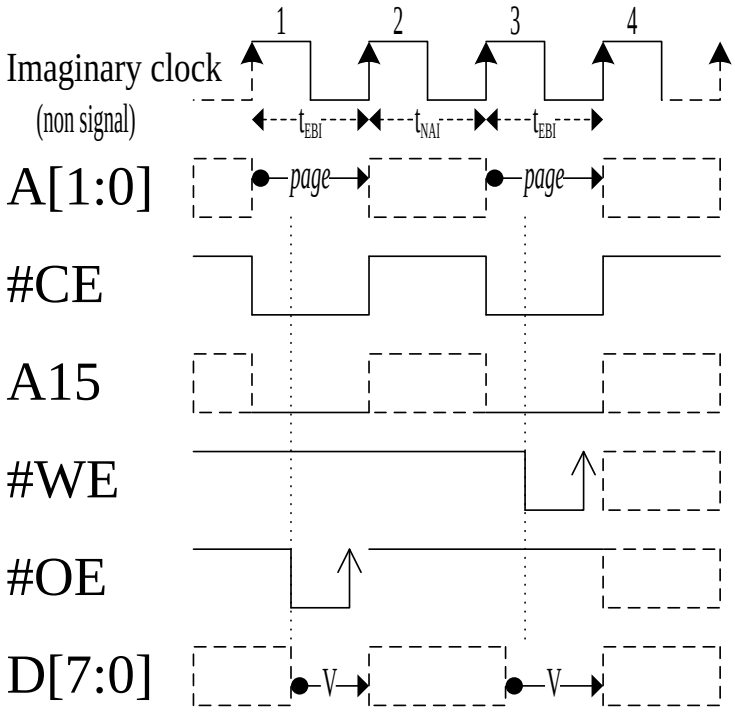
Chip Configuration

D[7:0]	A[2]=0, A[1:0]
Null 0	**Config page** 00: page 0

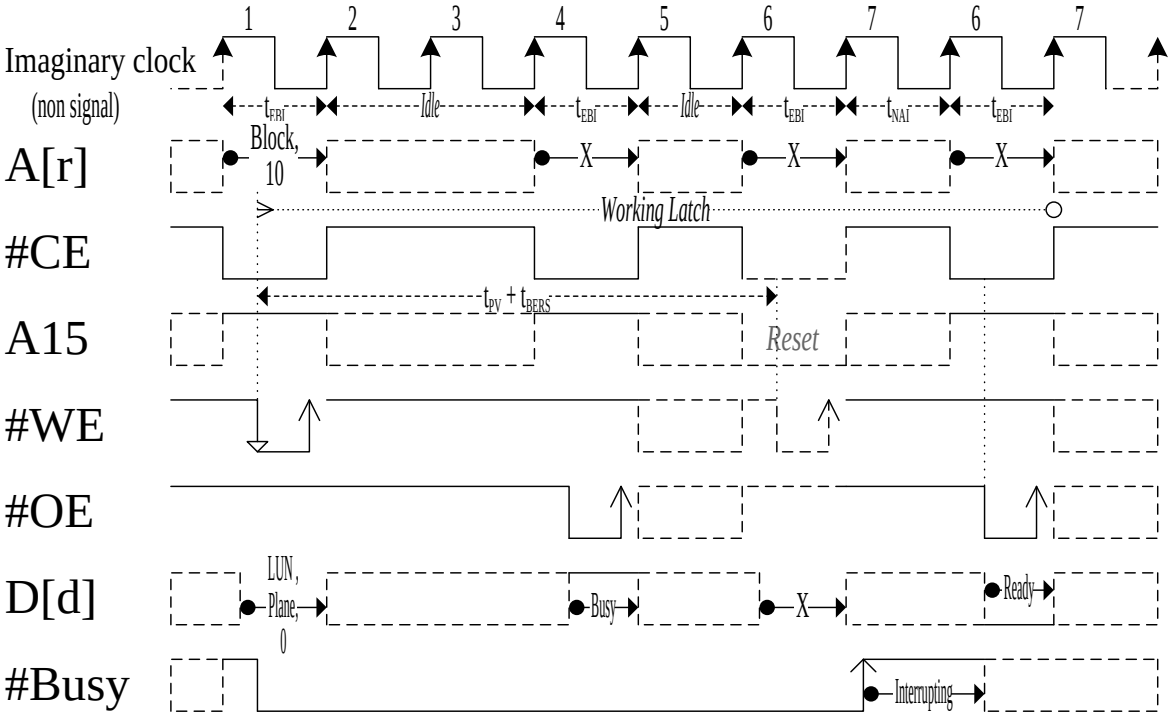
D[7:1]	D[0]	A[2]=0, A[1:0]
Null 0	**Erase or program reset** 0: finish (POR) 1: reset	**Config page** 11: page 3

Timing Diagram

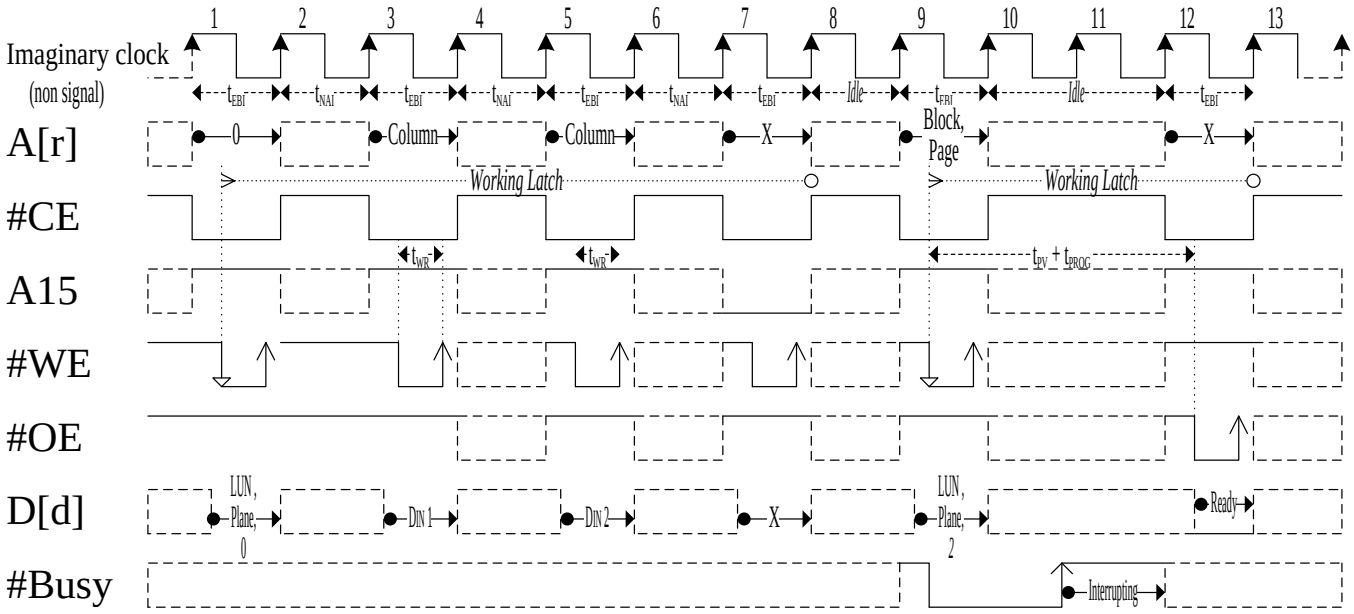
- Chip Information and Chip Configuration



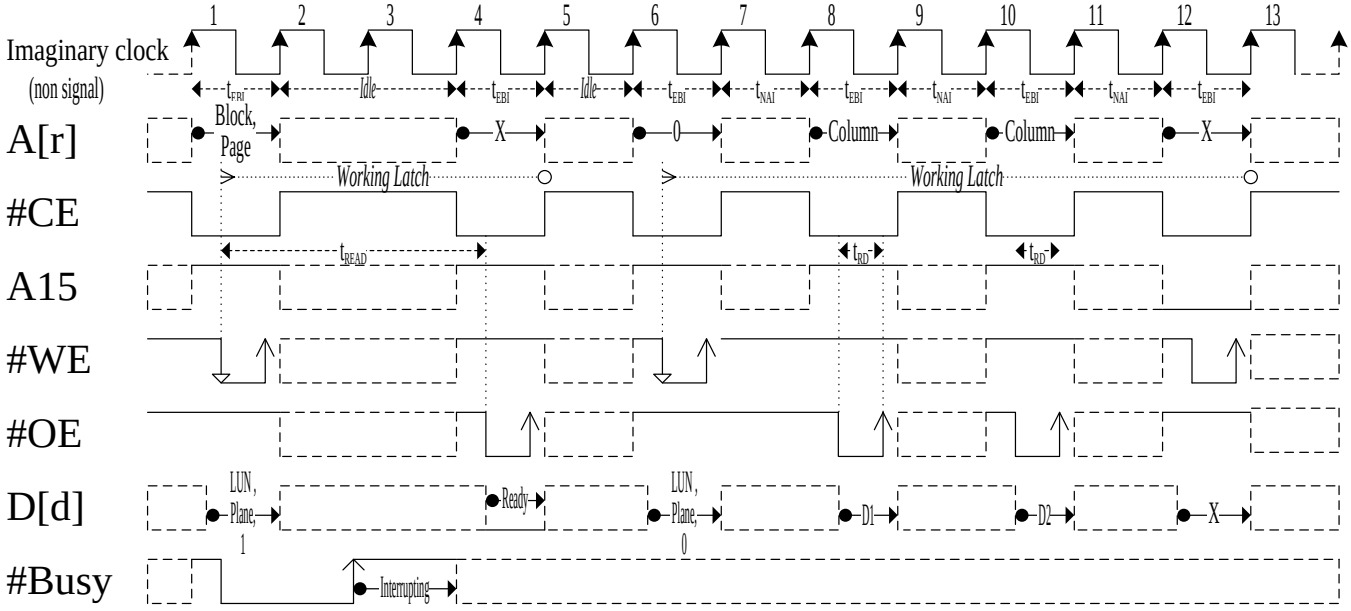
- Block Erase



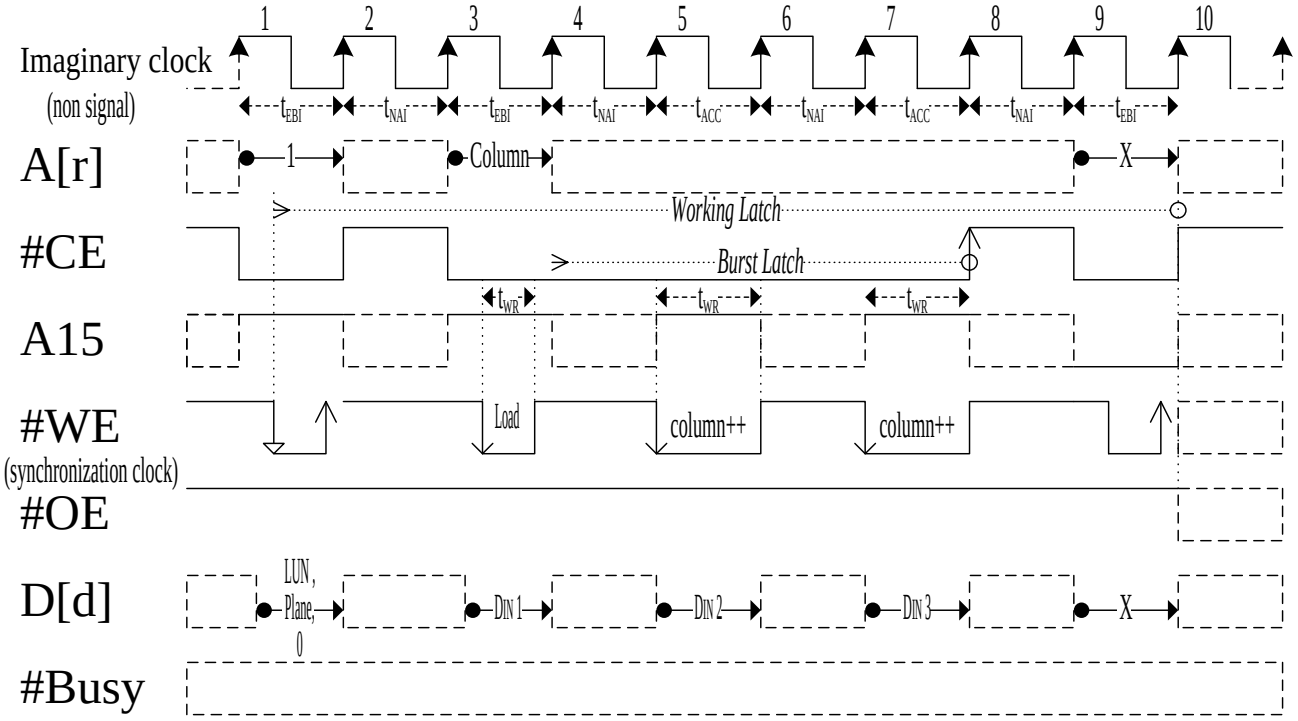
■ Random Write and Page Program



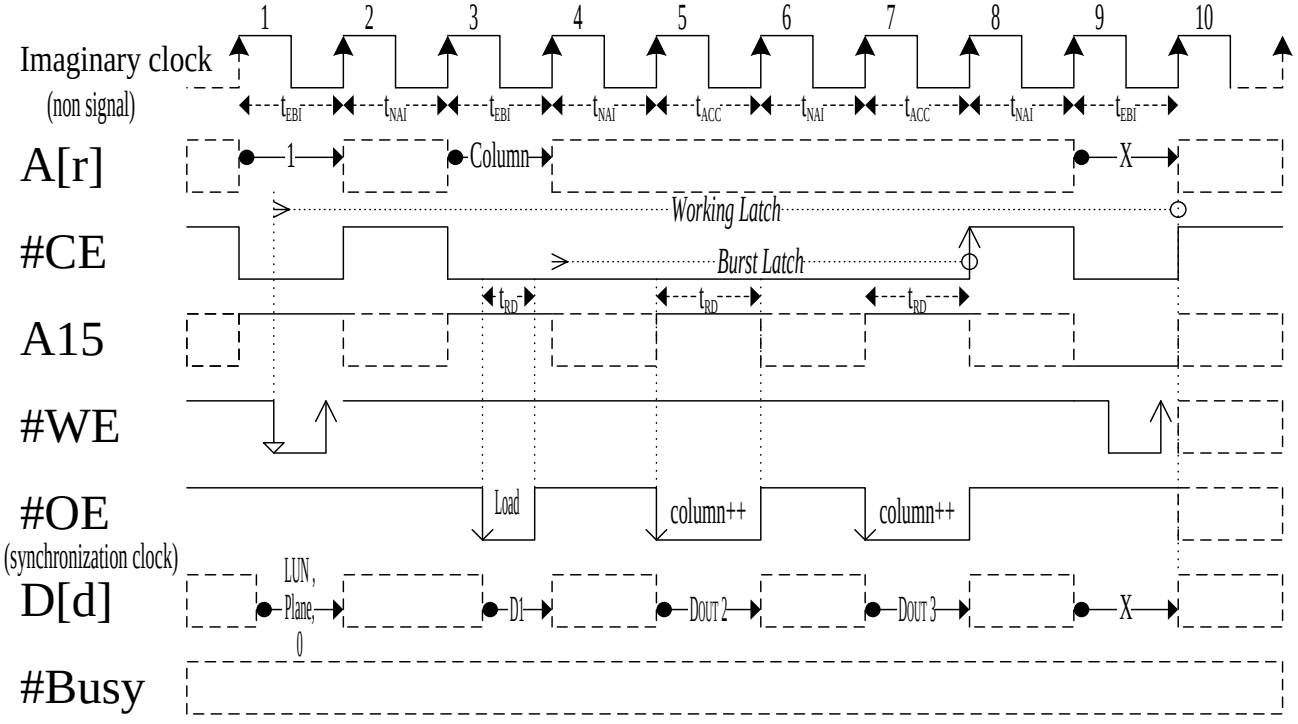
■ Page Read and Random Read



■ Synchronization Burst Write



■ Synchronization Burst Read



Release Note

Table of Release Note

Version	Release Date	Release Note
1.0	2020-05-11	First formal version.
1.1	2020-05-18	According to the asynchronous SRAM chip which can select data width is single byte or double byte, the package ball-out can add the #UB and #LB.
1.2	2020-07-27	To add SPMI DRAM versus DDR2 SDRAM.
1.3	2020-08-03	1. To beautify SPMI DRAM versus DDR2 SDRAM. 2. To beautify timing diagrams and correct symbols on them. 3. To correct the operation time of accessing. 4. To correct some error words.
1.4	2020-08-24	1. To define clearly, the symbols CK and #CK are reserved signals. 2. To rename the “Speed Write” becoming “Fast Write”. 3. To add a write mode in MRS, and remove the Fast Write from command set. 4. To rename the “Write” in timing diagram of SPMI DRAM. 5. To rename the “Operation Time of Accessing and Refreshing” in SPMI SRAM. 6. To change the number of the Fast Write in SPMI SRAM. 7. To rename the “SPMI NAND Flash Memory”. 8. To change the number of the Random Write in SPMI NAND. 9. To correct some symbols in timing diagram of SPMI NAND. 10. To add an approach of a bridge board.
1.5	2021-04-12	1. To correct the command set and the timing diagram of SPMI DRAM; and to exchange the read and write timing diagram (SPMI SRAM), by the way. 2. To modify the Platform Hardware Architecture. 3. To modify the architecture of SPMI DRAM, and SPMI SRAM.
1.6	2021-08-02	1. Fixed some bugs of all timing diagram. 2. Fixed command set of burst access. 3. Merge SPMI DRAM with SPMI SRAM.
1.7	2021-09-13	1. Fixed some bugs of all timing diagram. 2. Remove the power down command in SPMI DRAM. 3. Modify the Mode Register. 4. Modify the Operation Time of Accessing and Refreshing.
1.8	2021-09-20	1. Modify the command set and the function number in SPMI DRAM. 2. Modify the quantity of periodic refresh command. 3. Modify the function name in SPMI NAND.
1.9	2021-09-27	Modify the SDRAM bridges.
1.10	2021-11-22	Modify the SPMI DRAM versus [DDR-n] SDRAM.

1.11	2022-02-07	1. Fixed the figures (Platform Hardware Architecture, and SPMI DRAM versus [DDR-n] SDRAM). 2. Fixed the command set of SPMI DRAM.
2.0	2022-03-28	To upgrade SPMI DRAM and SPMI NAND. To reduce GPIO operation times (switching GPIO is usually slower).
3.0	2022-04-08	To upgrade SPMI DRAM and SPMI NAND. To remove all GPIO (it is not fast on advanced hardware and software platforms).
3.1	2022-07-25	1. To add EBI DRAM. 2. Fixed all of the Package Ball-out. 3. To beautify the Timing Diagram of EBI. 4. To beautify all of the Timing Diagram.
3.2	2022-08-29	1. To add DDR3 SDRAM package mapping table. 2. The ALE is no more an option on SPMI NAND. 3. To redefine the tDACC and tBACC, and tDACC is changed to tRACC. 4. To shift the location of Operation Time of Accessing.
3.3	2022-09-26	1. To add Simplified State Diagram. 2. Modify Chip Information.
3.4	2022-10-10	1. Modify the waveforms of burst write and burst read. 2. Modify the Simplified State Diagram.
3.5	2022-11-14	Fixed the definition of EBI. Fixed “The device refresh parameters”.
3.6	2023-01-12	Fixed the package mapping table. Fixed the formula of tRFC. Rename EtST to ST. Modify the Chip Information, and remove not needed fields.
4.0	2023-02-06	To add HSMBI DRAM.
4.1	2023-02-13	To add HSMBI Host Controller and IO.
4.2	2023-02-20	To change the wafer process to a low power activity. To add bank refresh mask for low power application.
4.3	2023-03-06	Redefine SPMI NAND.
4.4	2023-07-17	Modify some definitions (no technical changes).
4.5	2023-08-07	Bug fixed: the command set for auto refresh. Add pin: #RESET.